ScioSense

Datasheet

DS000586

AS6501

2-Channel Time-to-Digital Converter

v3-00 • 2020-May-19

Content Guide

1 General Description

The AS6501 is a high performance time-to-digital converter (TDC) frontend device. Highest measurement performance and highest data throughput is achieved on two channels, each on with LVDS stop inputs and LVDS serial outputs. High configuration flexibility and unlimited measurement range cover many applications. They range from portable handheld laser range equipment to ambitious time-of-flight measurements of highest performance, as e.g. done in medical imaging applications.

AS6501 calculates all stop measurements inside, proportional to the applied reference clock. Combinations of best single shot accuracy of 10 ps with lowest pulse-to-pulse spacing < 5ns and maximum data throughput rate of 70 MSPS per stop input are possible.

1.1 Key Benefits & Features

The benefits and features of AS6501, 2-Channel Time-to-Digital Converter, are listed below:

Figure 1:
Added Value of Using AS6501

Benefits	Features
• Simple data post-processing thanks to calibrated results	• 2 stop channels with serial 20 ns pulse-to-pulse spacing and maximum 35 MSPS • 1 combined channel with 5 ns pulse-to-pulse spacing and maximum 70 MSPS • Single shot accuracy 20 ps rms single shot resolution per channel or 10 ps rms with high resolution option • Unlimited measuring range 0 s to 16 s
• Event assignment thanks to reference clock index simplifies coincidence measurements • Easy pulse width measurements • High efficiency thanks high sample rate	• Differential reference clock input 2 MHz to 12.5 MHz • Inputs optional with LVDS (or CMOS level) • LVDS serial output per channel • 16-stage FIFO per channel • Automatic calibration to reference clock (no PLL or DLL) • SPI compatible 4-wire interface for configuration
• Compact design thanks to small package and low number of external components • Reduced cooling thanks to low power consumption	• Supply voltage 3.3 V • Power dissipation 60 mW to 260 mW • Standby current 60 µA • QFP48 package (7 mm x 7 mm)

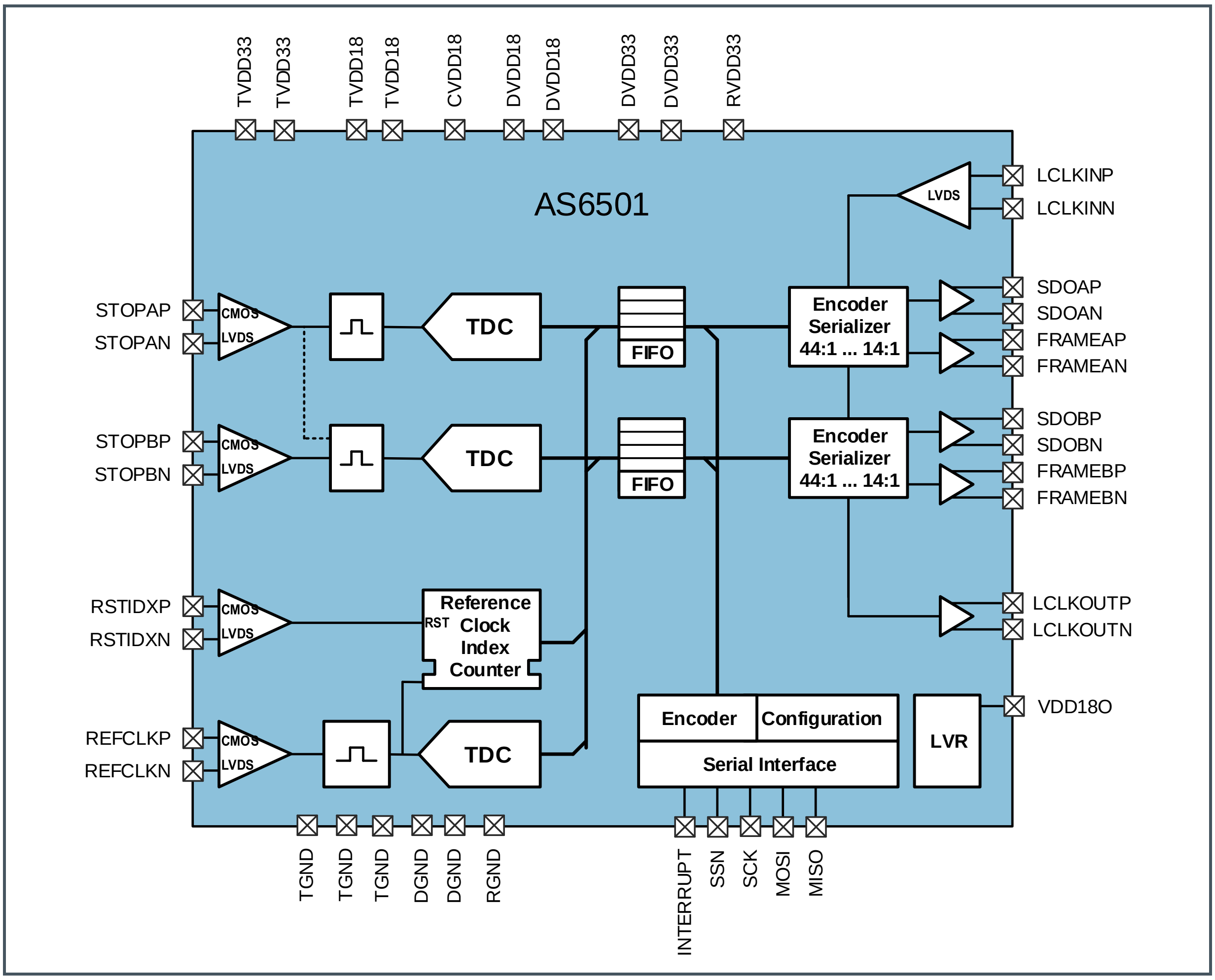
1.2 Applications

- Automated test equipment
- Laser range measurement
- Medical imaging
- Time-of-flight measurement
- Particle physics
- Lidar

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS6501



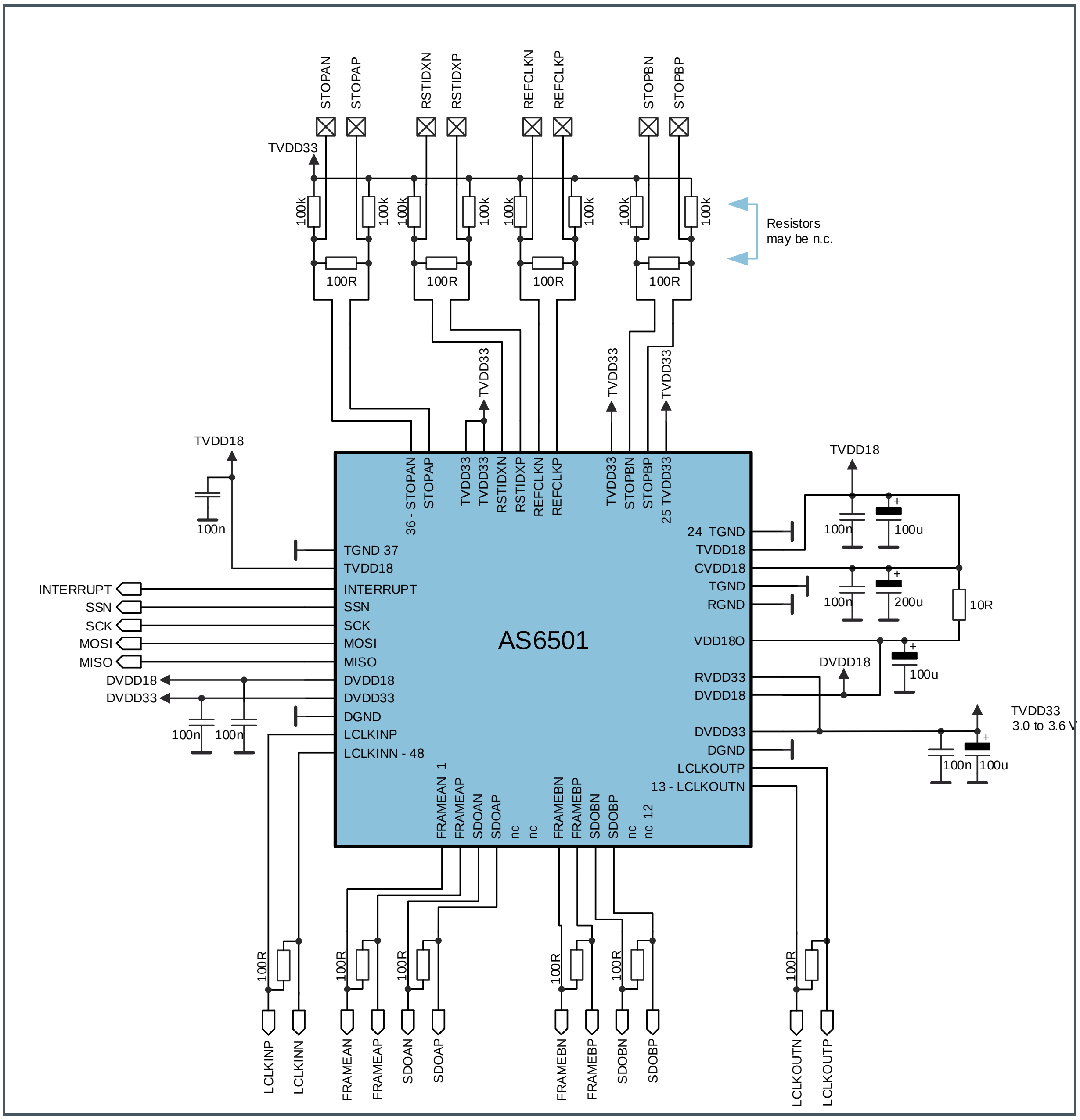
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS6501-FLQM	QFP48	AS6501	T&R	500 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
AS6501 QFP48



3.2 Pin Description

Figure 4:
Pin Description of AS6501 QFP48

Pin Number	Pin Name	Pin Type(1)	Description	Not Used
1	FRAMEAN	LVDS Output	Negative frame signal of stop channel A	Open
2	FRAMEAP	LVDS Output	Positive frame signal of stop channel A	Open
3	SDOAN	LVDS Output	Negative serial data output of stop channel A	Open
4	SDOAP	LVDS Output	Positive serial data output of stop channel A	Open
5, 6	NC		Not Connected	Open
7	FRAMEBN	LVDS Output	Negative frame signal of stop channel B	Open
8	FRAMEBP	LVDS Output	Positive frame signal of stop channel B	Open
9	SDOBN	LVDS Output	Negative serial data output of stop channel B	Open
10	SDOBP	LVDS Output	Positive serial data output of stop channel B	Open
11, 12	NC		Not Connected	Open
13	LCLKOUTN	LVDS Output	Negative serial clock output	Open
14	LCLKOUTP	LVDS Output	Positive serial clock output	Open
15	DGND	Power Supply	Ground for digital and IO units	
16	DVDD33	Power Supply	3.3V supply for digital and IO units	
17	DVDD18	Power Supply	1.8V supply for digital and IO units	
18	RVDD33	Power Supply	3.3V supply for linear voltage regulator	
19	VDD18O	Regulator Output	1.8V supply for digital and IO units, regulator output	
20	RGND	Power Supply	Ground for linear voltage regulator	
21	TGND	Power Supply	Ground for TDC	
22	CVDD18	Power Supply	1.8V positive supply for TDC	
23	TVDD18	Power Supply	1.8V positive supply for time front-end	
24	TGND	Power Supply	Ground for 1.8V time front-end supply	
25	TVDD33	Power Supply	3.3V positive supply for time front-end	
26	STOPBP	CMOS/LVDS Input	Positive stop input for channel B	TVDD33
27	STOPBN	LVDS Input	Negative stop input for channel B	TVDD33
28	TVDD33	Power Supply	3.3V positive supply for time front-end	

Pin Number	Pin Name	Pin Type(1)	Description	Not Used
29	REFCLKP	CMOS/LVDS Input	Positive clock signal of reference clock	TVDD33
30	REFCLKN	LVDS Input	Negative clock signal of reference clock	TVDD33
31	RSTIDXP	CMOS/LVDS Input	Positive reference index reset signal	TVDD33
32	RSTIDXN	LVDS Input	Negative reference index reset signal	TVDD33
33, 34	TVDD33	Power Supply	3.3V positive supply for time front-end	
35	STOPAP	CMOS/LVDS Input	Positive stop input for channel A	TVDD33
36	STOPAN	LVDS Input	Negative stop input for channel A	TVDD33
37	TGND	Power Supply	Ground for TDC	
38	TVDD18	Power Supply	1.8V positive supply for time front-end	
39	INTERRUPT	LVTTL output	SPI interrupt	
40	SSN	LVTTL Input	SPI slave select not + interface reset	
41	SCK	LVTTL Input	SPI serial clock	
42	MOSI	LVTTL Input	SPI serial data master out , slave In	
43	MISO	LVTTL Tristate	SPI serial data master in, slave Out	
44	DVDD18	Power Supply	1.8V supply for digital and IO units	
45	DVDD33	Power Supply	3.3V supply for digital and IO units	
46	DGND	Power Supply	Ground for digital and IO units	
47	LCLKINP	LVDS Input	Positive serial clock in	DVDD33
48	LCLKINN	LVDS Input	Negative serial clock in	DVDD33

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of AS6501

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD33	3.3V Supply Voltage to Ground	-0.5	4.0	V	Pin: DVDD33, TVDD33, RVDD33
VDD18	1.8V Supply Voltage to Ground	-0.5	2.2	V	Pin: DVDD18, TVDD18, CVDD18
	Voltage between ground pins	-0.3	+0.3	V	Pin: DGND, TGND, RGND
V_{iLVDS}	Voltage at differential input pins	-0.3	VDD33 + 0.3	V	Pin: STOPA, STOPB, REFCLK, RSTIDX, LCLKIN
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 1000		V	JS-001-2014
Temperature Ranges and Storage Conditions					
T_J	Operating Junction Temperature	-40	125	°C	
T_{STRG}	Storage Temperature Range	- 65	150	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100 % Sn)

5 Recommended Operation Conditions

Recommended operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Test conditions for guaranteed specification are expressly denoted.

Figure 6:
Recommended Operation Conditions of AS6501

Symbol	Pin	Description	Min	Typ	Max	Unit
Power-Supply						
VDD33	DVDD33, TVDD33, RVDD33	Supply Voltage	2.4	3.3	3.6	V
VDD18	DVDD18, TVDD18, CVDD18	Core Supply Voltage powered by integrated regulator, pin VDD18O	1.7	1.8	1.9	V
Temperature						
T_A		Operating free air temperature(1)	-40		125	°C
Reference & Stop Inputs						
$V_{ID,LVDS}$	STOPA, STOPB, REFCLK, RSTIDX	LVDS Differential Input Voltage	200			mV
$V_{IC,LVDS}$	STOPA, STOPB, REFCLK, RSTIDX	LVDS Common Mode Input Voltage	0.5 × $V_{ID,LVDS}$	1.25	2.2V to 0.5 × $V_{ID,LVDS}$	V
$V_{IL,CMOS}$	STOPA, STOPB, REFCLK, RSTIDX	CMOS Input Low Voltage			0.4	V
$V_{IH,CMOS}$	STOPA, STOPB, REFCLK, RSTIDX	CMOS Input High Voltage	VDD33 – 0.4			V
SPI-Interface						
V_{IL}	SCK, MOSI, SSN	Digital Input LOW Voltage			0.8	V
V_{IH}	SCK, MOSI, SSN	Digital Input HIGH Voltage	0.7 × VDD33			V
C_{LOAD}	INTERRUPT, MISO	Load Capacitance to Ground			20	pF
LVDS-Interface						
$V_{ID,LVDS}$	LCLKIN	LVDS Differential Input Voltage	200			mV
$V_{IC,LVDS}$	LCLKIN	LVDS Common Mode Input Voltage		1.25		V

Symbol	Pin	Description	Min	Typ	Max	Unit
R_{TERM}	SDOA, SDOB, FRAMEA, FRAMEB, LCLKOUT	Differential Termination Resistor for LVDS Outputs		100		Ohm
C_{LOAD}		Load Capacitance to Ground			5	pF

(1) Recommended Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Test conditions for guaranteed specification are explicitly denoted.

6 Typical Characteristics

The following test levels apply to all following characteristics:

Figure 7:
Test Levels

Test Level	Description
I	100% production tested.
II	100% production tested at 25°C and guaranteed by design and characterization testing
III	Parameter is guaranteed by design and characterization testing
IV	Sample tested
V	Parameter is a typical value only.

6.1 Converter Characteristics

General Conditions: VDD33 = 3.3 V; VDD18 = 1.8 V; T_A = 0 °C to 80 °C.

Figure 8:
Converter Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Accuracy of Time Measurement							
RMS	Single-shot RMS resolution	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	IV		20 15 10	30 20 15	ps
INL	Integral non-linearity		IV			20	ps
DNL	Differential non-linearity		V		5		ps
	No missing code	At time quantization level	III	Assured			
	Channel to channel isolation	At same times measured	IV		20	100	ps
	Offset error	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	V		100 150 200		ps

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
	Offset error temperature drift	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	IV		0.5 1 1.5	3	ps/K
Switching Performance							
t_{CONV}	Converter latency	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III			20 50 100	ns
	Peak conversion rate	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III			50 20 10	MSPS
	Maximal read-out rate SDR: LCLK=250MHz DDR: LCLK=250MHz SPI : SCK = 50MHz	Data bit width: 14-Bit 14-Bit Opcode + 16-Bit	III			17.8 35.7 2.1	MSPS
	Maximal read-out rate SDR: LCLK=250MHz DDR: LCLK=250MHz SPI : SCK = 50MHz	Data bit width: 44-Bit 44-Bit Opcode + 48-Bit	III			5.6 11.3 0.9	MSPS

6.2 Power Supply Characteristics

General Conditions: VDD33 = 3.3 V; VDD18 = 1.8 V; T_A = 0 °C to 80 °C.

Figure 9:
Power Supply Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Supply Voltage							
t_{VDD18O}	Delay from power-up of RVDD33 to TVDD18O, CVDD18O, DVDD18O stable	C_{load} = 100 µF	V			100	ms
$P_{TOT,MIN}$	Minimum total power dissipation	CMOS inputs and SPI read f_{REFCLK} = 5 MHz conversion rate 1MSPS	V		60		mW
$P_{TOT,MAX}$	Maximum total power	LVDS inputs and outputs f_{REFCLK} = 10 MHz $f_{STOPA,B}$ = 50 MHz f_{LCLK} = 250 MHz	V		260		mW

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Detailed Current Consumption							
$I_{DVDD18,REFCLK}$	Core current into REFCLK	f_{REFCLK} = 5 MHz	V		2		mA
$I_{DVDD18,STOP}$	Current per stop channel	Stop rate = 0.5 MHz	V		0.5		mA
I_{CVDD18}	Current with activated TDC core		V		14		mA
$I_{DVDD33,LVDS-IN}$ $I_{TVDD33,LVDS-IN}$	Current per LVDS input buffer		III		2	6	mA
$I_{DVDD33,LVDS-OUT}$	Current per LVDS output buffer	R_{TERM} = 100 Ω	III		5	10	mA
I_{DDQ}	Quiescent current mainly by I_{RVDD33}	LVDS inputs tied to VDD33	II		60	100	µA
I_{LKG}	Input leakage current	LVDS, CMOS, Digital	II	-5		1	µA

6.3 Reference Clock and Stop Input Requirements

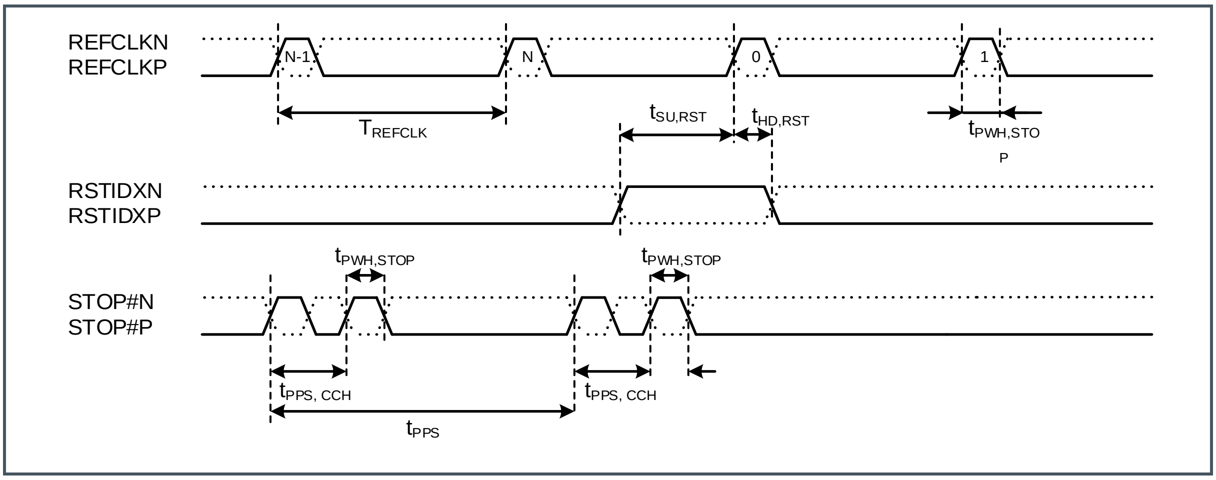
General Conditions: VDD33 = 3.3 V; VDD18 = 1.8 V; T_A = 0 °C to 80 °C; VID = 200mV; VIC = 1.25 V; VIL = 0 V; VIH = 3.3 V

Figure 10:
Clock and Input Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
f_{REFCLK}	Reference clock frequency	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III	2 2 2	5 5 5	12.5 12.5 10.0	MHz
T_{REFCLK}	Reference clock period		III	83	200	500	ns
	Reference clock jitter		V			100	ps
	Reference clock stability	No requirement					
$t_{PWH,STOP}$	Minimum pulse width	LVDS CMOS	III	2 10			ns
t_{PPS}	Minimum pulse-to-pulse spacing	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III	20 50 100			ns

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
$t_{PPS,CCH}$	Minimum pulse-to-pulse spacing for a single pair of pulses	CHANNEL_COMBINE = 1	III	5			ns
$t_{SU,RST}$	Setup Time from RSTIDX to REFCLK		III	5			ns
$t_{HD,RST}$	Hold Time from RSTIDX to REFCLK		III	5			ns
t_{PIN_ENA}	Pin Activation Time from configuration of PIN_ENA… to valid data	Pins: RSTIDX, REFCLK, STOPA/B	III	200			µs
t_{POR}	Delay between power-on or initialization reset and next communication	Delay between power-on or initialization reset and next communication	III	100			µs

Figure 11:
Timing Symbols and Parameters



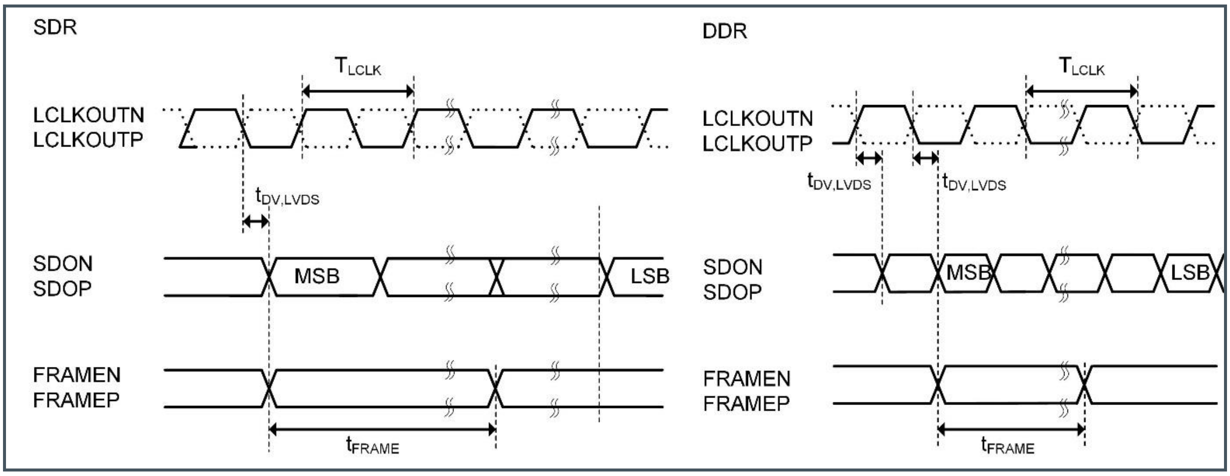
6.4 LVDS Data Interface Characteristics

General Conditions: VDD33 = 3.3 V; VDD18 = 1.8 V; T_A = 0 °C to 80 °C; VID = 200mV; VIC = 1.25 V

Figure 12:
LVDS Interface Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Electrical Characteristics							
$V_{OD,LVDS}$	LVDS differential output voltage	R_L = 100 Ω, C_L = 5 pF	III	200			mV
$V_{OC,LVDS}$	LVDS common mode output voltage	R_L = 100 Ω, C_L = 5 pF	III	1.125	1.25	1.375	V
t_{PIN_ENA}	Pin activation time from configuration PIN_ENA_LVDS to valid data at pin	Pin: LCLKIN, LCLKOUT, SDOA/B, FRAMEA/B	III			200	µs
Timing Characteristics							
t_{SYNC}	Synchronization latency	SDR DDR	III		6 3		Clock
t_{FRAME}	Frame length	SDR DDR	III		8 4		Clock
f_{LCLK}	LVDS clock frequency SDR/DDR		III	10		250	MHz
	LVDS clock duty cycle		III	45	50	55	%
	Path delay LCLKIN to LCLKOUT, SDOA/B, FRAMEA/B		III		5	10	ns
$t_{DV,LVDS}$	Data valid after active clock edge	lvds_data_valid _adjust = 1	III		0		ns

Figure 13:
LVDS Timing Symbols and Parameters



6.5 Serial Communication Interface

General Conditions: VDD33 = 3.3 V; VDD18 = 1.8 V; T_A = 0 °C to 80 °C; VIL = 0V; VIH = 3.3 V

Figure 14:
Serial Communication Interface Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Electrical Characteristics							
V_{OL}	Digital Output LOW Voltage	I_O = 2 mA	III			0.3	mV
V_{OH}	Digital Output HIGH Voltage	I_O = 2 mA	III	DVDD33 -0.3			mV
Timing Characteristics							
f_{SCK}	Serial clock frequency	C_L = 5 pF	III			50	MHz
$t_{PWH,SCK}$	Serial clock pulse width HI state		III	10			ns
$t_{PWL,SCK}$	Serial clock pulse width LO state		III	10			ns
$t_{PWH,SSN}$	SSN pulse width between write cycles		III	10			ns
$t_{SU,SSN}$	SSN setup time after SCK falling		III	20			ns

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
$t_{HD,SSN}$	SSN hold time before SCK rising		III	20			ns
$t_{SU,MOSI}$	Data setup time prior to clock edge		III	5			ns
$t_{HD, MOSI}$	Data hold time after clock edge		III	5			ns
$t_{DV,MISO}$	Data valid after rising clock edge		III	8			ns
$t_{ZX,MISO}$	HighZ to output time		III	8			ns
$t_{XZ,MISO}$	Output to HighZ time		III	8			ns

Figure 15:
Write and Incremental Write

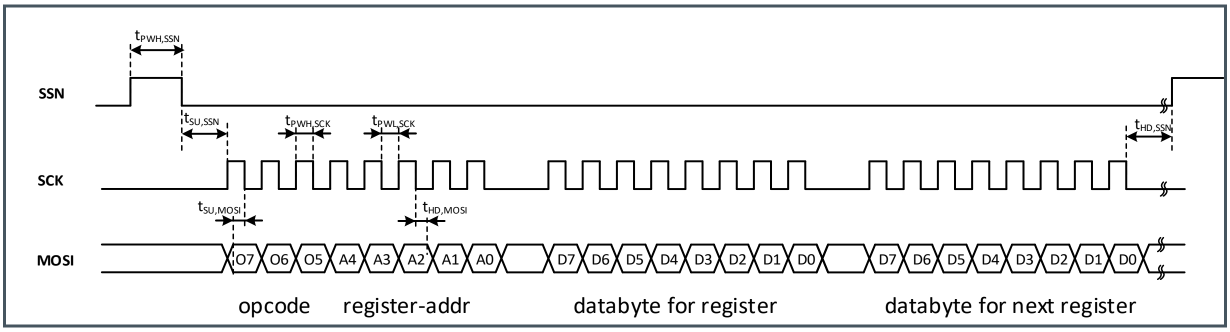
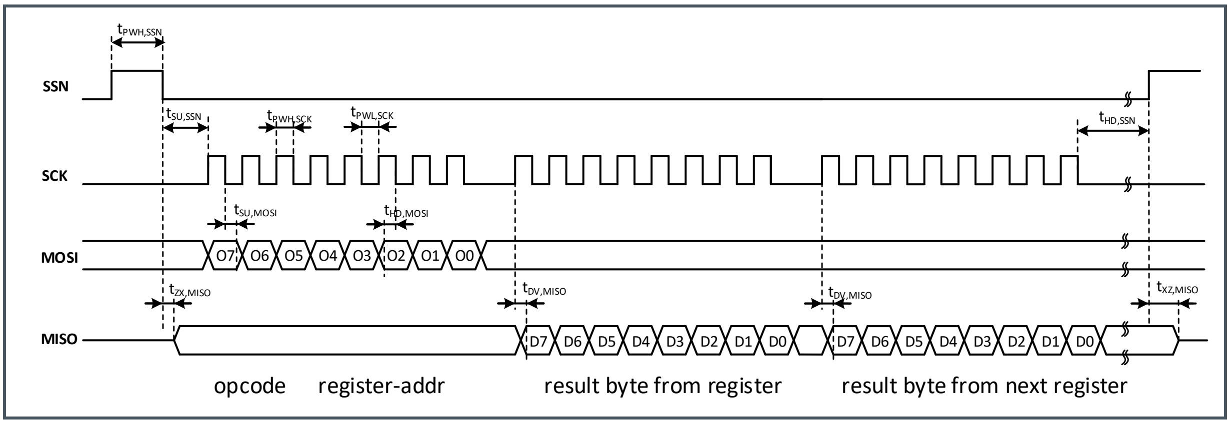


Figure 16:
Read and Incremental Read



6.6 Typical Operating Characteristics

Figure 17:
STOP, HIGHRES 4x, Histogram 100000 Values

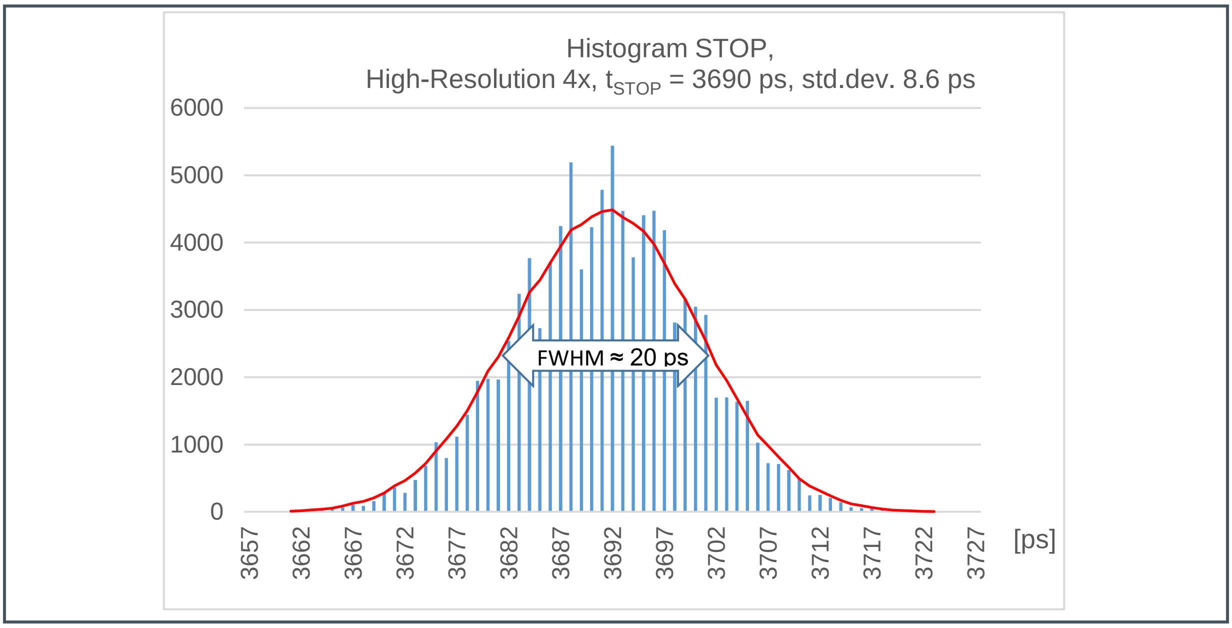


Figure 18:
STOPB – STOPA, HIGHRES 4x, Histogram 100000 Values

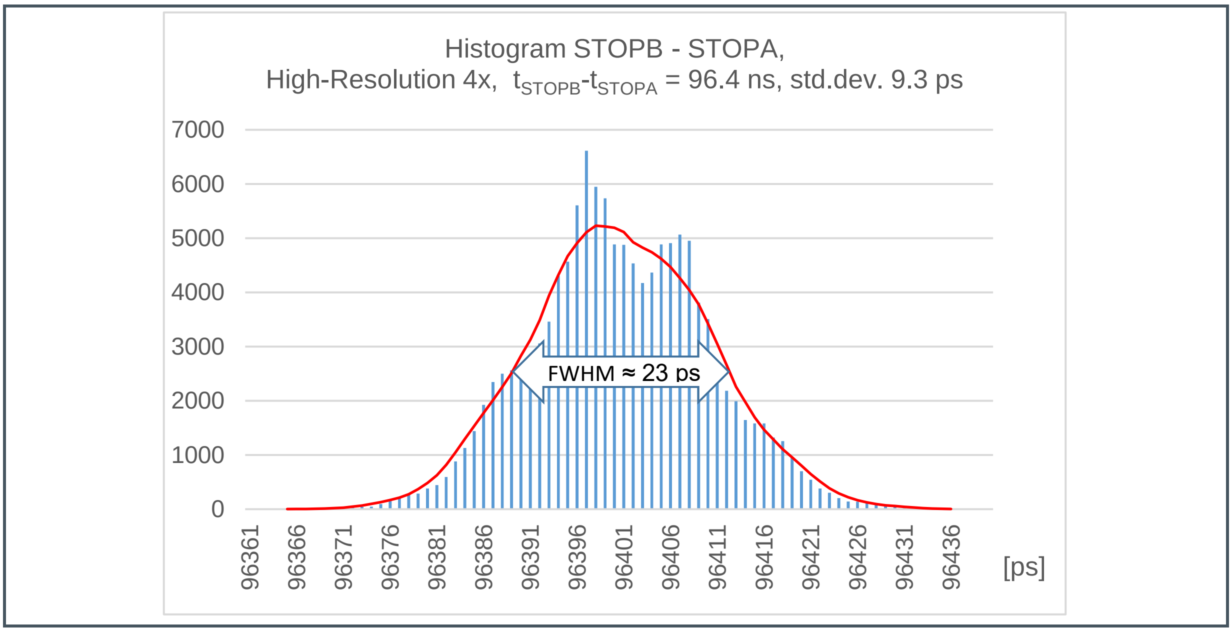


Figure 19:
STOP – REFCLK, HIGHRES Off, Histogram 100000 Values

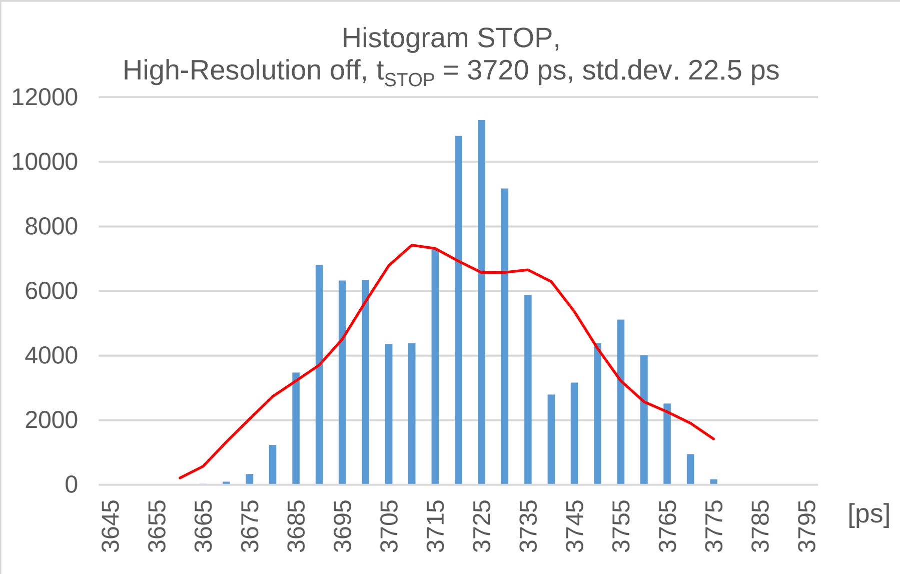


Figure 20:
STOPB – STOPA, HIGHRES Off, Histogram 100000 Values

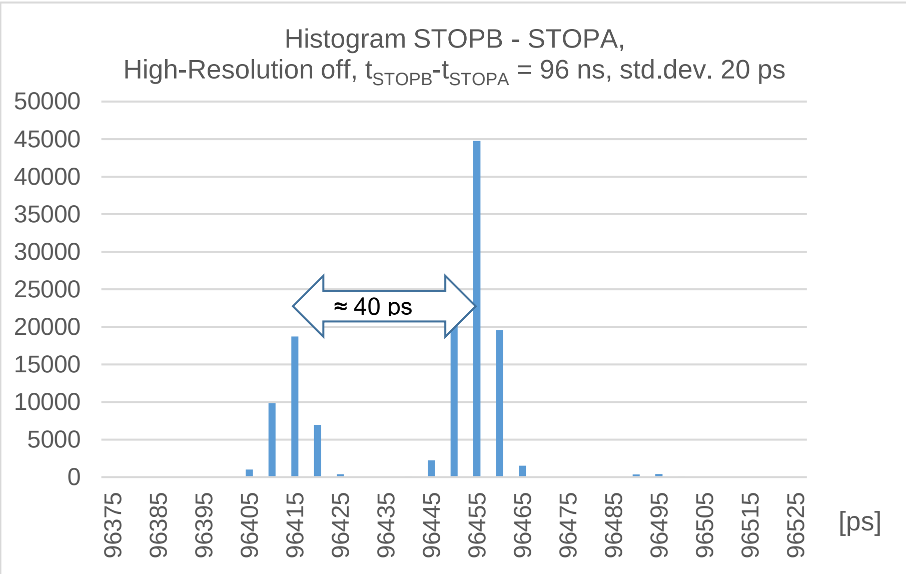
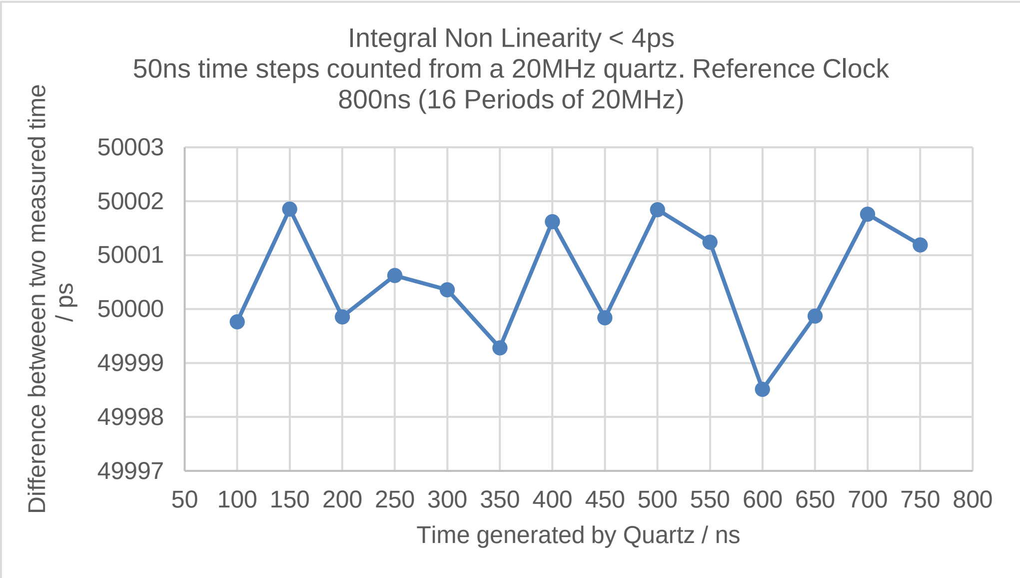


Figure 21:
Integral Non-Linearity



7 Register Description

7.1 Register Overview

The configuration registers are organized in 17 addresses of one byte. All configuration registers are accessible via the SPI interface with the spiopc_write_config and spiopc_read_config. The result read registers are organized in 12 addresses of one byte. All result read registers are accessible via the SPI interface with spiopc_read_result. Users can read and write register individually or with an incremental access.

Figure 22:
Configuration Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0	CFG0	PIN_ ENA_ RSTIDX	Fixed value: (0b)	PIN_ ENA_ LVDS_ OUT	PIN_ ENA_ REFCLK	Fixed value: (0b)	PIN_ ENA_ STOPB	Fixed value: (0b)	PIN_ ENA_ STOPA
1	CFG1	HIGH_ RESOLUTION		CHANNEL_ COMBINE		Fixed value: (0b)	HIT_ ENA_ STOPB	Fixed value: (0b)	HIT_ ENA_ STOPA
2	CFG2	BLOCK WISE_ FIFO READ	COMMON_ FIFO_ READ	LDVS_ DOUBLE_ DATA_ RATE	STOP_DATA_BIT WIDTH		REF_INDEX_BITWIDTH		
3	CFG3	REFCLK_DIVISIONS (Lower byte)							
4	CFG4	REFCLK_DIVISIONS (Middle byte)							
5	CFG5	Fixed value: (0000b)				REFCLK_DIVISIONS (Upper bits)			
6	CFG6	Fixed value: (110b)			LVDS_ TEST_ PATTERN	Fixed value: (0000b)			
7	CFG7	Fixed value: (01b)		LVDS_DATA_VALID_ ADJUST		Fixed Value: (0011b)			
8	CFG8	Fixed value: (10100001b)							
9	CFG9	Fixed value: (00010011b)							
10	CFG10	Fixed value: (00000000b)							
11	CFG11	Fixed value: (00001010b)							
12	CFG12	Fixed value: (11001100b)							
13	CFG13	Fixed value: (11001100b)							
14	CFG14	Fixed value: (11110001b)							
15	CFG15	Fixed value: (01111101b)							
16	CFG16	Fixed value: (00000b)					CMOS_ INPUT	Fixed value: (00b)	

All register are read/write with 0 as default value, besides registers 13 and 14 with 5 as default value. The fixed values are assigned by **ScioSense**: Unless otherwise suggested, they should be set as shown in this table.

Figure 23:
Result Register Overview

Addr	Name	<D7>
0 to 7		n.c.
8	CHANNELA	REFERENCE INDEX CHANNEL A BYTE #3
9		REFERENCE INDEX CHANNEL A BYTE #2
10		REFERENCE INDEX CHANNEL A BYTE #1
11		STOP RESULT CHANNEL A BYTE #3
12		STOP RESULT CHANNEL A BYTE #2
13		STOP RESULT CHANNEL A BYTE #1
14 to 19		n.c.
20	CHANNELB	REFERENCE INDEX CHANNEL B BYTE #3
21		REFERENCE INDEX CHANNEL B BYTE #2
22		REFERENCE INDEX CHANNEL B BYTE #1
23		STOP RESULT CHANNEL B BYTE #3
24		STOP RESULT CHANNEL B BYTE #2
25		STOP RESULT CHANNEL B BYTE #1

7.2 Detailed Register Description

7.2.1 CFG0 Register (Address 0)

The PIN_ENA registers activate the LVDS input or output drivers of the related pins. Main purpose of PIN_ENA is cutting of current consumption of differential LVDS buffers to nearly zero. But also with CMOS input levels the pins have to be activated accordingly. Unused inputs has to be tied to VDD33.

Figure 24:
CFG0 Register

Addr: 0		CFG0		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
0	PIN_ENA_STOPA	0	RW	Activation on stop event input pin STOPA 0:= Stop input pins not active 1:= Stop input pins active
1	Fixed value:	0	RW	(0b)

Addr: 0		CFG0		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
2	PIN_ENA_ STOPB	0	RW	Activation on stop event input pin STOPB 0:= Stop input pins not active 1:= Stop input pins active
3	Fixed value:	0	RW	(0b)
4	PIN_ENA_ REFCLK	0	RW	0:= REFCLK input pins not active 1:= REFCLK input pins active
5	PIN_ENA_ LVDS_OUT	0	RW	0:= All LDVS output pins disabled 1:= Activation of LCLK and LCLKOUT pins. Activation of SDOA/B and FRAMEA/B, depends further on CHANNEL_COMBINE and PIN_ENA
6	Fixed value:	0	RW	(0b)
7	PIN_ENA_ RSTIDX	0	RW	0:= Deactivation of reference clock index counter reset pin 1:= Activation of reference clock index counter reset pin

7.2.2 CFG1 Register (Address 1)

Figure 25:
CFG1 Register

Addr: 1		CFG1		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
0	HIT_ENA_ STOPA	0	RW	0:= Stop events are internally rejected. The pin enabling of STOPA is not affected. 1:= Stop events are internally accepted and processed. Normal working condition
1	Fixed value:	0	RW	(0b)
2	HIT_ENA_ STOPB	0	RW	0:= Stop events are internally rejected. The pin enabling of STOPB is not affected. 1:= Stop events are internally accepted and processed. Normal working condition
3	Fixed value:	0	RW	(0b)
4, 5	CHANNEL_ COMBINE	0	RW	The two stop channels may be combined for improved pulse pair resolution or higher conversion rate. 00b := Normal operation with two independent stop channels 01b := “Pulse distance” Stop events at STOPA are measured alternatingly by stop channels A & B 10b := “Pulse width” The rising edges at STOPA are measured by stop channel A, the falling edges at STOPA are measured by stop channel B

Addr: 1		CFG1		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
6, 7	HIGH_ RESOLUTION	0	RW	A stop event is internally delayed, measured several times and summed up in order to one result to increase the time resolution. 00b := 0 (Off): standard resolution with minimal pulse-to-pulse spacing. 01b := 1 (2x): A stop event is measured twice 10b := 2 (4x): A stop event is measured four times

7.2.3 CFG2 Register (Address 2)

Figure 26:
CFG2 Register

Addr: 2		CFG2		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
[2:0]	REF_INDEX_ BITWIDTH	o	RW	Bit width of reference clock index in LVDS output (not applicable to SPI data readout). 000b := 0 bit, no data out 001b := 2 bits 010b := 4 bits 011b := 8 bits 100b := 16 bits 101b := 24 bits 110b := 6 bits 111b := 12 bits
3, 4	STOP_DATA_ BITWIDTH	0	RW	Bit width of the stop result in LVDS output. Bit width should be sufficient to represent the REFCLK_DIVISIONS configuration value (not applicable to SPI data readout). 00b := 14 Bits → max of REFCLK_DIVISIONS = 2^{14}-1 01b := 16 Bits → max of REFCLK_DIVISIONS = 2^{16}-1 10b := 18 Bits → max of REFCLK_DIVISIONS = 2^{18}-1 11b := 20 Bits → max of REFCLK_DIVISIONS = 2^{20}-1
5	LVDS_DOUBLE_ DATA_RATE	0	RW	0:= Single Data Read (SDR): The LVDS data clocked out on rising edges of LCLK-OUT 1:= Double Data Read (DDR): The LVDS data are clocked on both edges of LCLK-OUT

Addr: 2		CFG2		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
6	COMMON_ FIFO_READ	0	RW	0:= Off LVDS: Operation with two independent stop channels SPI: INTERUPT pin is set to zero, as soon as one FIFOs does have a value.OFF. 1:= On LVDS: All active frame pins are set simultaneous as soon as all related FIFOs have values. SPI: INTERUPT pin is set to zero, as soon as all active FIFOs have value. In combination with BLOCKWISE_READ this option guaranties successive measurements in parallel on all stop channels
7	BLOCKWISE_ FIFO_READ	0	RW	0:= OFF, Operation with standard FIFO function 1:= Data output (LVDS or SPI) is not started before a channel FIFO is full. Once FIFO is full, measurement is not restarted before FIFO is completely read-out. This option guaranties successive measurements at high stop event rate or slow read-out speeds (e.g. SPI)

7.2.4 CFG3, CFG4, CFG5 Registers (Addresses 3 to 5)

These registers combine for a 20-bit value.

Figure 27:
CFG3, CFG4, CFG5 Registers

Addr: 3		CFGRG3		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
0 to 7	REFCLK_DIVISIONS Lower 8 bits	0	RW	Defines a LSB at the output interface as fraction of the reference clock period. The most convenient way is applying a LSB of 1ps by configuring REFCLK_DIVISIONS to the picosecond value of the reference clock period
Addr: 4		**CFGRG4**		
0 to 7	REFCLK_DIVISIONS Middle 8 bits	0	RW	See above
Addr: 5		**CFGRG5**		
0 to 3	REFCLK_DIVISIONS High 4 bits	0	RW	See above
4 to 7	Fixed value:	0	RW	(0000b)

7.2.5 CFG6 Register (Address 6)

Figure 28:
CFG6 Register

Addr: 6		CFG6		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
0 to 3	Fixed value:	0	RW	(0000b)
4	LVDS_TEST_PATTERN	0	RW	0:= Normal operation of LVDS outputs 1:= LVDS interface continuously outputs the following test patterns. All stop events are ignored. Reference index = 111100001100110010101010bin (=15781034dec) Stop result = 000010101010110011110000bin (=699632dec) Depending on the configuration of the output format width (REF_INDEX_BITWIDTH, STOP_DATA_BITWIDTH) only the corresponding lower bits are transmitted
5 to 7	Fixed value:	0	RW	(000b)

7.2.6 CFG7 Register (Address 7)

Figure 29:
CFG7 Register

Addr: 7		CFG7		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
0 to 3	Fixed value:	0	RW	(0000b)
4, 5	LVDS_DATA_VALID_ADJUST	0	RW	Adjustment of the data valid time at the LVDS output interface. 00b := - 160 ps 01b := 0 ps 10b := +160 ps 11b := +320 ps
6, 7	Fixed value:	0	RW	(00b)

7.2.7 CFG8 to CFG15 Register (Addresses 8 to 15)

For registers 8 to 15 use the default fixed values as shown in the Register Overview.

7.2.8 CFG16 Register (Address 16)

Figure 30:
CFG16 Register

Addr: 16		CFG16		
Bit	**Bit Name**	**De-fault**	**Ac-cess**	**Bit Description**
0, 1	Fixed value:	0	RW	(00b)
2	CMOS_INPUT	0	RW	Input voltage levels of STOPA and STOPB, REFCLK, RSTIDX are selected as CMOS or LVDS 0:= Differential LVDS input level. 1:= Single ended CMOS input level Also with CMOS input level the pins have to be activated with according PIN_ENA-configuration
3 to 7	Fixed value:	0	RW	(00000b)

7.2.9 CHANNELA Result Register (Addresses 8 to 13)

ChannelA register is made of 6 bytes. Three bytes for the reference index REFID, three bytes for the time stamp:

Figure 31:
CHANNELA Register

Address	Name	Description	Format
8	REFID1	REFERENCE INDEX CH1 BYTE #3	REFID = 2^{16}×BYTE#3 + 2^{8}×BYTE#2 + BYTE#1
9		REFERENCE INDEX CH1 BYTE #2	
10		REFERENCE INDEX CH1 BYTE #1	
11	TSTOPA	STOP RESULT CH1 BYTE #3	TSTOP = 2^{16}×BYTE#3 + 2^{8}×BYTE#2 + BYTE#1
12		STOP RESULT CH1 BYTE #2	
13		STOP RESULT CH1 BYTE #1	

REFID is the reference index of the preceding reference clock edge.

TSTOP is the ratio of the internal measured times of t_{STOP} over t_{REF} scaled by the configured REFCLK_DIVISONS. For details see section Time Measurements and Results.

7.2.10 CHANNELB Result Register (Addresses 20 to 25)

ChannelA register is made of 6 bytes. Three bytes for the reference index REFID, three bytes for the time stamp:

Figure 32:
CHANNELB Register

Address	Name	Description	Header row left aligned
20	REFID3	REFERENCE INDEX CH3 BYTE #3	REFID = 2^{16}×BYTE#3 + 2^{8}×BYTE#2 + BYTE#1
21		REFERENCE INDEX CH3 BYTE #2	
22		REFERENCE INDEX CH3 BYTE #1	
23	TSTOPB	STOP RESULT CH3 BYTE #3	TSTOP = 2^{16}×BYTE#3 + 2^{8}×BYTE#2 + BYTE#1
24		STOP RESULT CH3 BYTE #2	
25		STOP RESULT CH3 BYTE #1	

REFID is the reference index of the preceding reference clock edge.

TSTOP is the measured time as ratio of the internal measured times of t_{STOP} over t_{REF} scaled by the configured REFCLK_DIVISONS. For details see section Time Measurements and Results.

8 Detailed Description

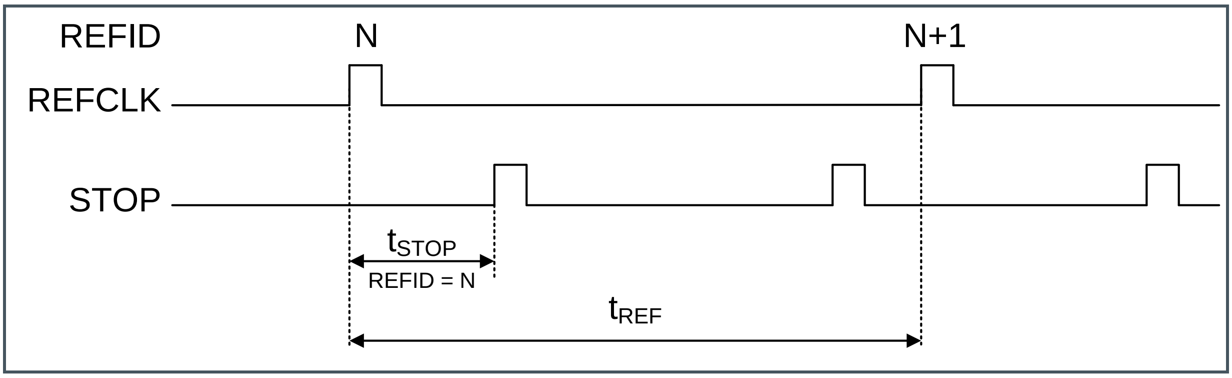
8.1 Time Measurements and Results

8.1.1 Measurements of AS6501

The reference clock is the framework for all time measurements. The clock pulses are measured continuously by the TDC as time reference point for stop pulses and as internal reference period. The measurement of the stop events always refers to the preceding reference clock. Additionally, the reference clock is counted continuously and the actual count is assigned as reference index to a stop pulse.

- t_{REF} is the internal TDC measurement of the reference clock period
- t_{STOP} is the internal TDC measurement of a stop to the preceding reference clock
- REFID is the index of reference period where the measured stop occurred

Figure 33:
AS6501 Time Measurement



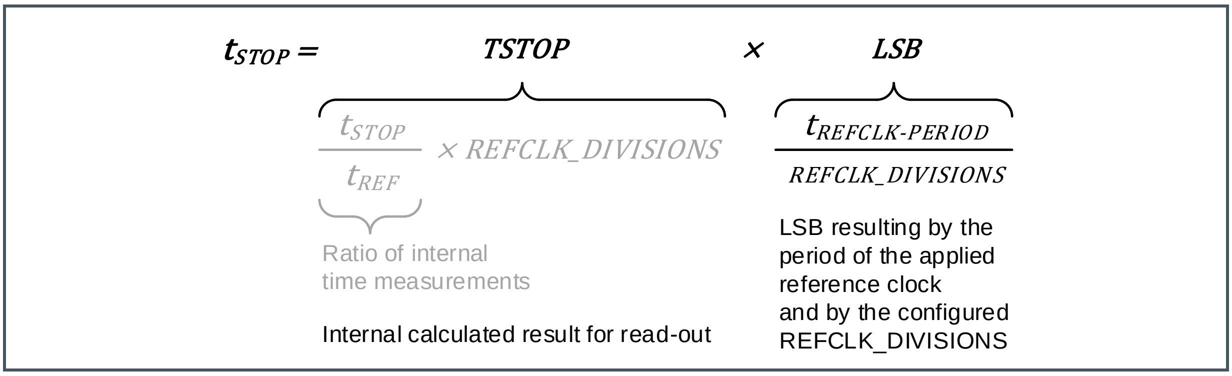
8.1.2 Output Results

Each stop generates a dataset that consists of two values TSTOP and REFID:

REFID is the reference index of the preceding reference clock pulse to TSTOP. The reference index is necessary to indicate the relationship of stop pulses that belong to different reference clock periods. The maximum length of the reference index is 20 bits.

TSTOP is the ratio of the internal measured times of t_{STOP} over t_{REF} scaled by the configured REFCLK_DIVISONS. The readout result TSTOP is always less than configured REFCLK_DIVISONS. The resulting LSB at the output interface should be chosen much lower than the single shot resolution of AS6501. For details, see chapter Coding of Results. Suitable values are e.g. 1 ps, 5 ps or 10 ps.

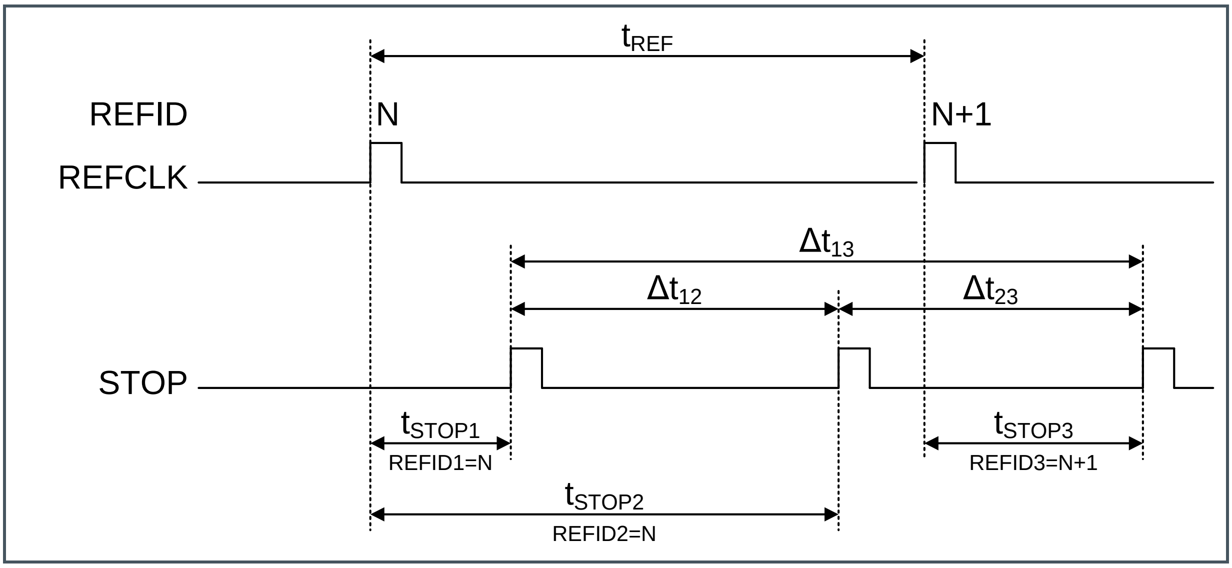
Figure 34:
Time Calculation



8.1.3 Calculation of Time Differences

The results of the AS6501 are the time intervals from stop event pulses to the preceding reference clock pulses. In many applications, the time difference between stop event pulses is desired. This happens e.g. in case of a quartz as a reference clock. Depending on the application and the measurement setup, several approaches are possible to calculate the time between two stops in the connected microprocessor or FPGA.

Figure 35:
Calculating Time Differences



GENERAL APPROACH

On the output interface, either SPI or LVDS, both data REFID and TSTOP are available. With these data, it is possible to calculate time differences between stops. The maximum time difference depends on the bit width of the reference index (see also chapter Maximum Time Differences).

Δt_{13} = (TSTOP3 – TSTOP1) + (REFID3 - REFID1) * REFCLK_DIVISIONS

In two special cases it is not necessary to readout the REFID:

- **STOPS IN THE SAME REFERENCE CLOCK PERIOD**

In applications where stops occur always in the same reference period, it is not necessary to read out the reference index. It is sufficient to read out just the stop results and to calculate the difference:

Δt_{12} = TSTOP2 – TSTOP1 if REFID2 = REFID1

- **TIME DIFFERENCE SMALLER THAN REFERENCE CLOCK**

In applications where the measured time difference Δt is always smaller than the reference clock period TREF but not necessarily in the same reference clock period, it is often sufficient to read out just the stop results without the reference index by distinguishing positive and negative time difference:

Δt_{23} = (TSTOP3 – TSTOP2) if TSTOP3 – TSTOP2 > 0

Δt_{23} = (TSTOP3 – TSTOP2) + REFCLK_DIVISIONS if TSTOP3 – TSTOP2 < 0

8.2 Resolution

8.2.1 RMS-Resolution versus Effective Resolution

The RMS resolution of a TDC is the root-mean-square-value of a set of single shot time measurements. TDC do not have an obvious full scale definition, as the time they are measuring is unlimited. Therefore, the definition of an effective resolution in number of bits likewise in ADC is not feasible.

8.2.2 High Resolution

For achieving best single-shot RMS resolution, AS6501 offers a complete integrated solution. During the initial sampling, the stop event is internally delayed and sampled again, after the first sample was stored in the FIFO. All samples of one stop event are averaged inside of the AS6501 and occur as one result with lower conversion noise at the output interface. With HIGH_RESOLUTION it is possible to configure internal 2 or 4 samples of one event. Due of the internal delay and the multiple samples the conversion latency t_{conv} and the pulse-to-pulse spacing t_{PPS} increase as well as the maximum FIFO_DEPTH decreases. In order to compensate these drawbacks, it is possible to use HIGH_RESOLUTION with both CHANNEL_COMBINATION modes and to achieve the excellent pulse-to-pulse spacing of channel combination mode, doubled FIFO depth per stop input and higher resolution.

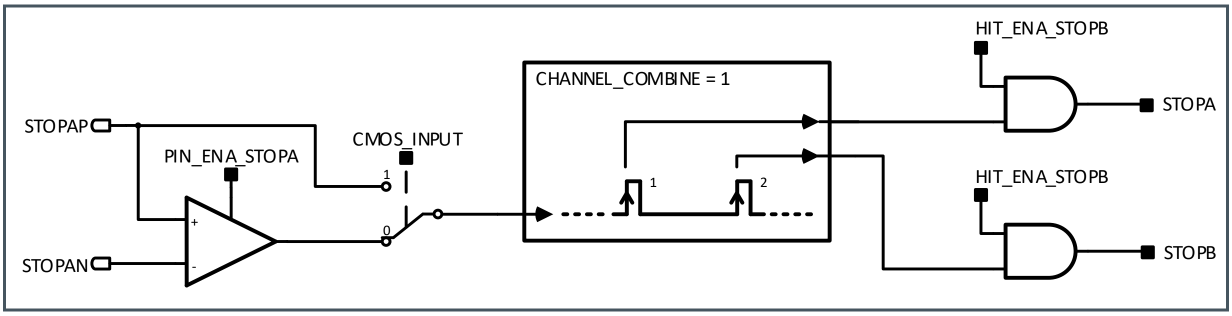
8.3 Combining Two Stop Channels

8.3.1 Channel Combination for Low Pulse-to-Pulse Spacing

With CHANNEL_COMBINE set to “PULSE_SPACING”, the two stop channels A & B are connected to one input pin STOPA. The stop events at the input pin are distributed alternatingly between the combined channels. Readout is indicated via FRAME or INTERRUPT pins when both channels have results in their FIFO. The advantage of combining channels lies in improved pulse-to-pulse spacing

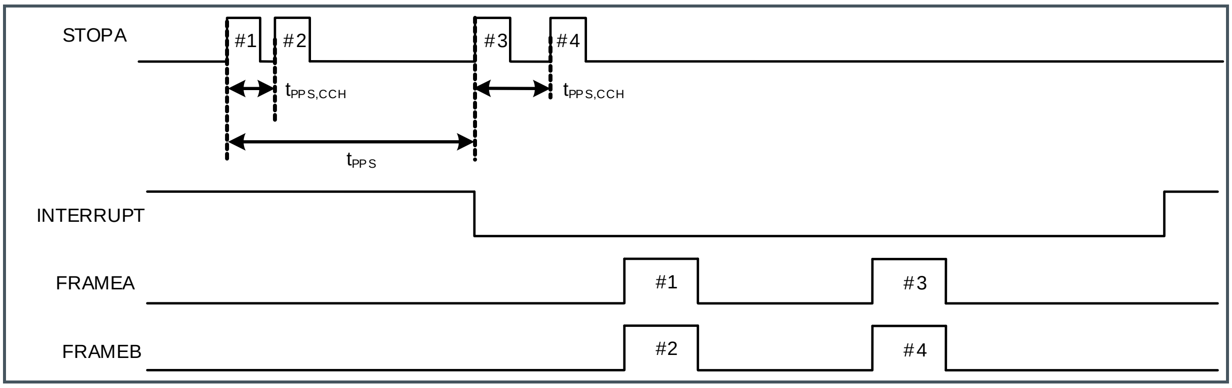
- Excellent pulse-to-pulse spacing
- Doubled FIFO depth per stop input pin
- Higher burst storage capability
- Doubled LVDS readout rate per stop input pin
- HIGH_RESOLUTION is applicable

Figure 36:
Channel Combination Low Pulse-to-Pulse Spacing



The outstanding low pulse-to-pulse spacing $t_{PPS,CCH}$ is achievable only for a single pulse pair. After a pulse pair, the regular pulse-to-pulse spacing t_{PPS} must be awaited, before capturing the next pulse becomes possible. Measurements with HIGH_RESOLUTION will increase the regular pulse-to-pulse spacing but the low pulse-to-pulse spacing $t_{PPS,CCH}$ is not affected.

Figure 37:
Channel Combination Low Pulse-to-Pulse Spacing



Information

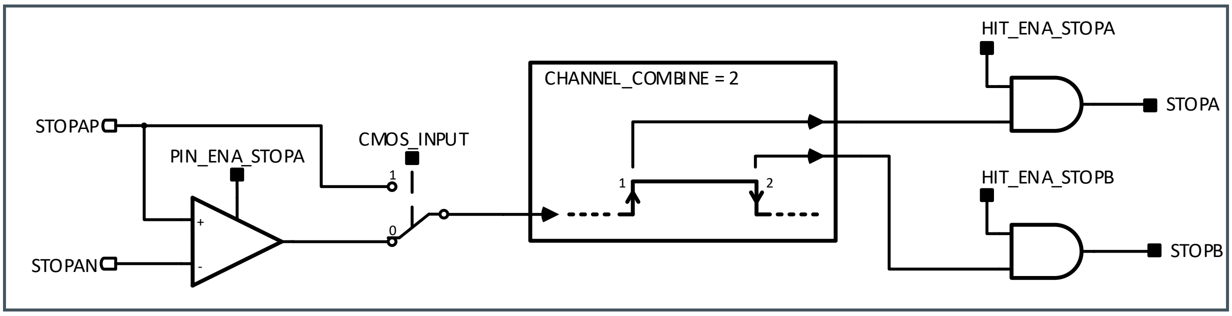
- With LVDS outputs the FRAME pins of combined channels are active together.
- SPI readout of combined channel pairs is permitted only pairwise like CHA-CHB-CHA-CHB-.
  But it is not permitted to read one channel twice like CHA-CHA-CHB-CHB-.

8.3.2 Channel Combination for Pulse Width Measurement

With CHANNEL_COMBINE set to "PULSE_WIDTH" the two internal stop channels A & B are connected to one input pin STOPA. The rising edges are measured by channel A, falling edges are measured by channel B. Readout starts on both channels simultaneous when a rising and falling edge was measured.

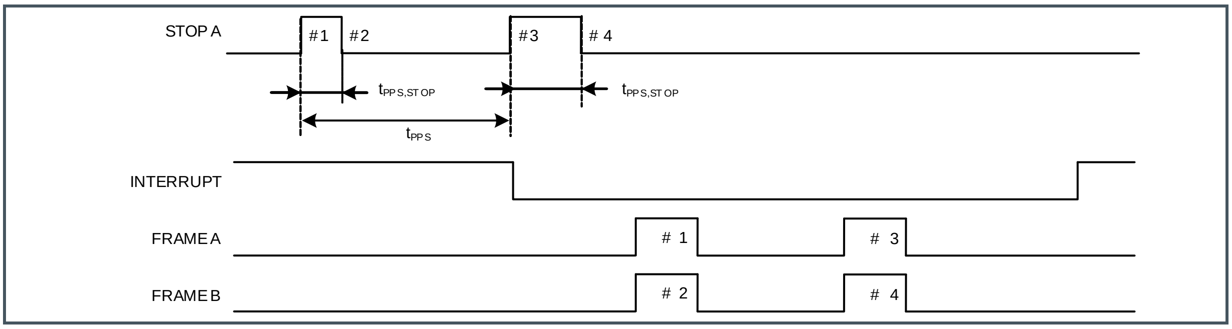
HIGH_RESOLUTION or COMMON_FIFO_READ is fully applicable

Figure 38:
Channel Combination Pulse Width Measurement



Note: For internal processing reasons, after the conversion latency t_{PPS} the next pulses can be captured earliest. Measurements with HIGH_RESOLUTION will increase the conversion latency but minimum pulse width $t_{PWH,STOP}$ is not affected.

Figure 39:
Channel Combination Pulse Width Measurement

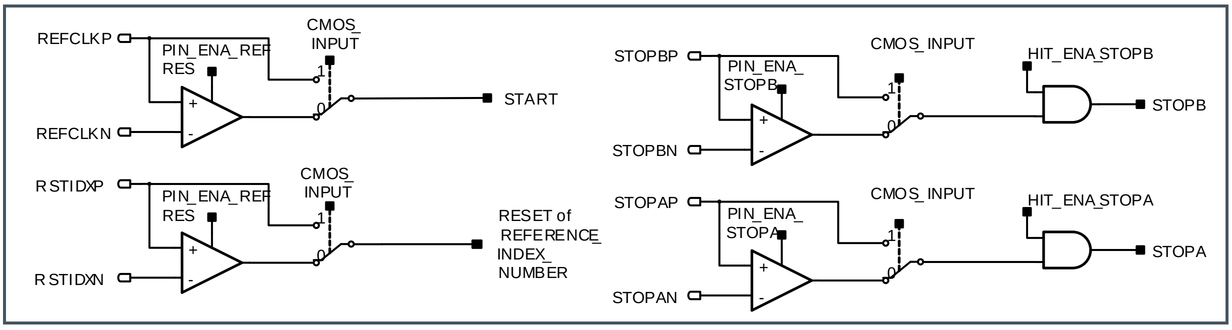


- With LVDS output the FRAME pins of combined channels are active together.
- SPI readout of combined channel pairs is permitted only pairwise like CHA-CHB-CHA-CHB-. But it is not permitted to read one channel twice like CHA-CHA-CHB-CHB-.

8.4 Input Pins for Time Measurement

The following diagram show the relevant input pins for the reference and the stops.

Figure 40:
Input Circuitry



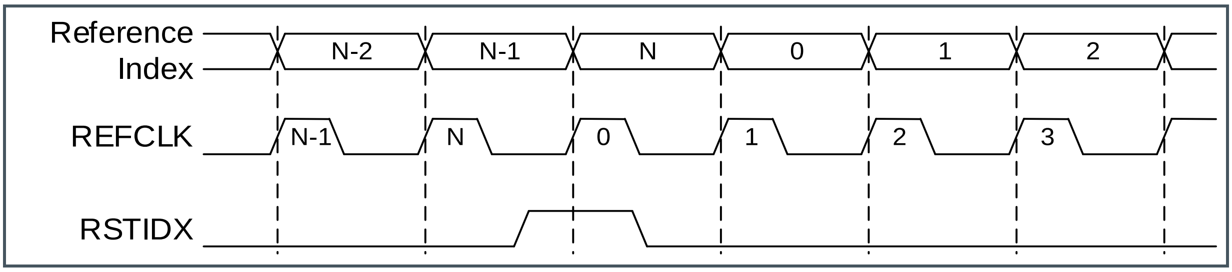
8.4.1 REFCLKP/N: Reference Clock Input

The reference clock serves as universal time base. Due to internal averaging, the phase jitter of the reference clock is non-critical. The accuracy and drift of the reference clock also does not affect the proper working of AS6501 itself. But it will directly affect the quality of the time measurement results.

8.4.2 RSTIDXP/N: Reference Index Counter Reset

With pin RSTIDX the internal counter for the reference index is set back to zero. This option may simply the overview on the reference index in the output data stream. RSTIDX is applied synchronously to the reference clock for at least a single period. After release of RSTIDX, one reference clock cycle passes before stop events are assigned with zero as reference index. The pin has to be activated with PIN_ENA_RSTIDX.

Figure 41:
Reference Index Counter Reset



8.4.3 STOPAP/N, STOPBP/N: Stop Channels

Inputs for the stop signals. The positive edges of the stop signals are measured versus the preceding reference clock edge.

The chip has two independent stop channels. With CHANNEL_COMBINE variations of this normal operation mode can be achieved.

8.4.4 Input Levels, CMOS or LVDS

All input pins, STOPA and STOPB, REFCLK and RSTIDX can be switched in common to CMOS input levels with CMOS_INPUT configuration. Tie the unused negative inputs to TVDD33.

Figure 42:
CMOS-LVDS General Circuit

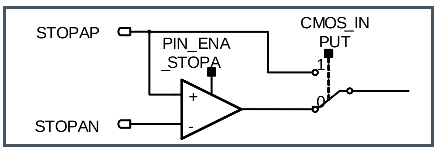


Figure 43:
LVDS (CMOS_INPUT=0):

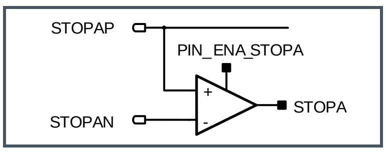
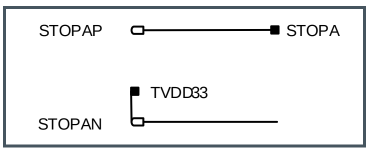


Figure 44:
CMOS (CMOS_INPUT=1):



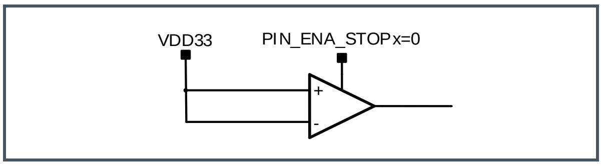
- Termination of differential LVDS input pins

There is no integrated termination. It is necessary to place termination resistors on the PCB near to the input pins. The default termination for LVDS signals is to have single 100 Ω resistors between the differential lines.

- Connecting unused LVDS inputs

Any kind of unused LVDS inputs (e.g. STOPA to STOPB, REFCLK, RSTIDX, LCLKIN) have to be pulled up to VDD33 and disabled by setting PIN_ENA to zero. Unused channels should also be switched off with HIT_ENA_STOPA or HIT_ENA_STOPB.

Figure 45:
Unused LVDS



- Software enable (HIT_ENA_STOPA/B)

Setting the configuration bits HIT_ENA_STOPA, HIT_ENA_STOPB applies a software enable for stop channels A and B.

- Pin ENABLE (PIN_ENA_XXX)

The pin enable registers PIN_ENA_STOPA and PIN_ENA_STOPB, PIN_ENA_REFCLK and PIN_ENA_RSTIDX activate the LVDS input or output drivers of the related pins. Main purpose of PIN_ENA is cutting of current consumption of unused differential LVDS buffer to nearly zero. But also with CMOS_INPUTs the pin need to be activated. In case of the LVDS output interface, PIN_ENA_STOPA and PIN_ENA_STOPB enable also the according LVDS output drivers.

8.5 LVDS Output Interface

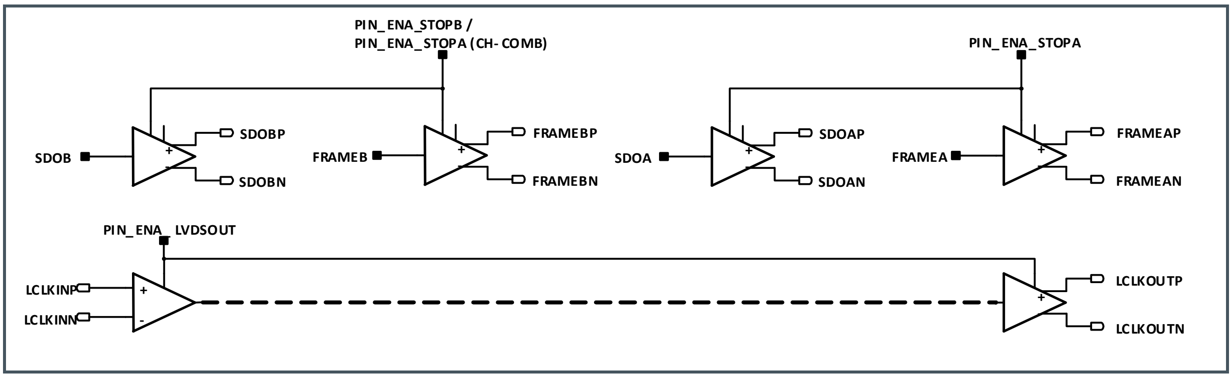
8.5.1 Digital Output Interface

Each stop channel has its own serial interface with a data output SDO pin and a FRAME pin to indicate the MSB. Data output is supported on falling edges (SDR, single data read) or rising and falling edges (DDR, double data read). The operating clock is looped from LCLKIN through the chip to LCLKOUT pin. The data at SDO and FRAME pins have stable timing relation a $t_{DV,LVDS}$ to LCLKOUT. The FRAME indicate the first 8 bits of an output sequence. On the SDO pin the reference index is output first, and the stop result follows that. The bit width of both results is configurable by STOP_DATA_BITWIDTH and REF_INDEX_BITWIDTH. With careful configuration data overhead can be avoided in favor of higher conversion rates.

8.5.2 Output Setup and Configuration:

LVDS output interface is activated configuring LVDS_ENA_LVDSOUT =1. The clock at the input LCLKIN is looped through the chip to pins LCLKOUT. The phase of SDO and FRAME pins are in stable relation to LCLKOUT. The SDO and FRAME pins needed for output are activated according to the configuration of PAD_ENA_STOPA to PAD_ENA_STOPB and CHANNEL_COMBINE.

Figure 46:
LVDS Outputs



8.5.3 LVDS Output Buffers

The LVDS output buffers SDOA, SDOB, FRAMEA, FRAMEB, and LCLKOUT are designed for 200mV voltage swing with external 100 Ω termination.

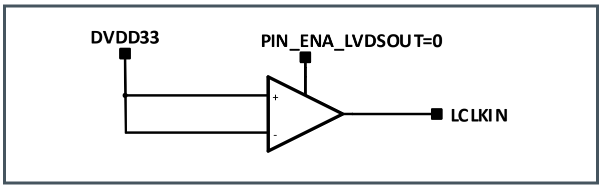
Unused LVDS output buffers can be left unconnected.

8.5.4 Differential LCLKIN Input

Termination: No integrated termination resistors are provided. A termination resistor of 100 Ohm should be placed near the input pin.

Connection of unused LCLKIN input: LCLKIN input has to be pulled up to VDD33 and disabled by configuring PIN_ENA_LVDS to zero.

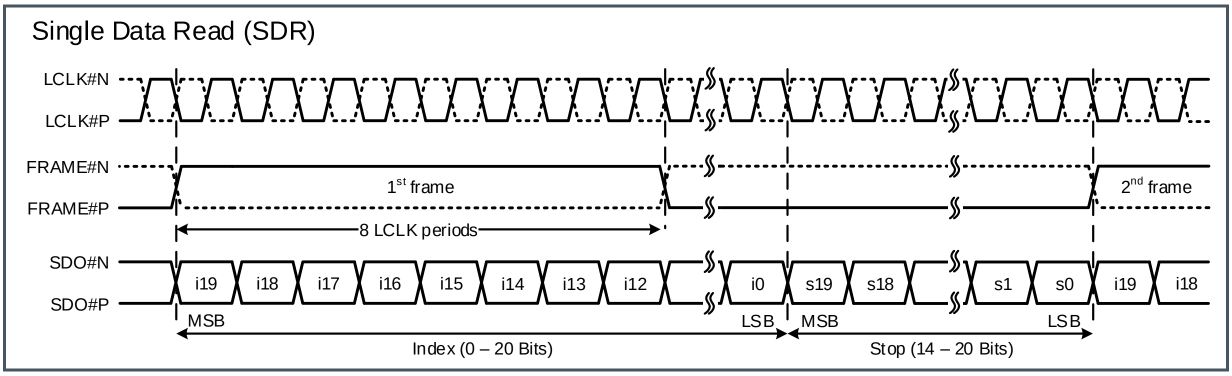
Figure 47:
LCLKIN Input



8.5.5 LVDS Single Data Read Output Interface (SDR)

In single data read mode (LVDS_DOUBLE_DATA_RATE = 0) the data and frame bits are clocked on the falling edge of LVDS output clock LCLKOUT. The data bits are stable during the following rising edge of LCLKOUT.

Figure 48:
LVDS Outputs SDR



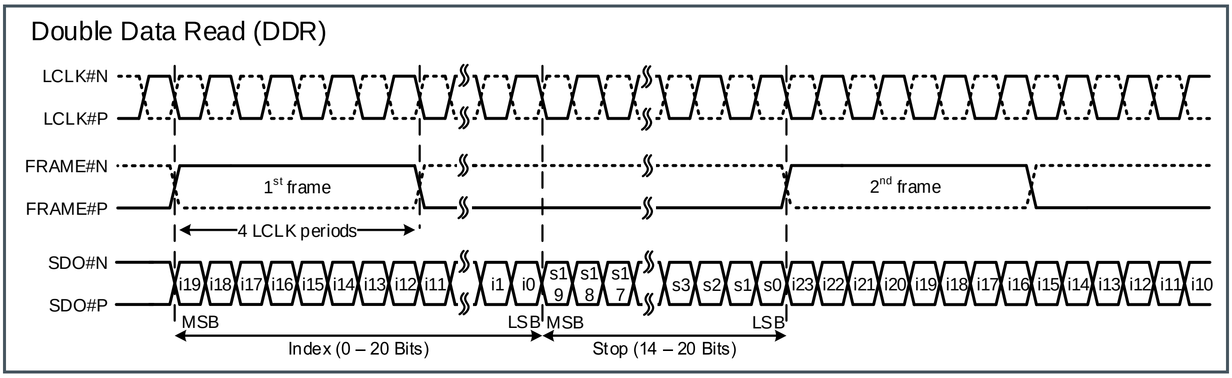
Information

Bit width of the reference index and the stop result is configured by STOP_DATA_BITWIDTH and REF_INDEX_BITWIDTH

8.5.6 LVDS Double Data Read Output Interface (DDR)

With double data read mode the readout rate is doubled or alternatively the LVDS clock frequency can be halved with constant readout rate. The data and frame bits are clocked on rising and falling edges of LCLKOUT. Both bits, data and frame, are delayed by $t_{DV,LVDS}$ to LCLKOUT in order to grant sufficient hold time for the receiving device. With configuration parameter LVDS_DATA_VALID_ADJUST the delay can be adjusted for all LVDS outputs in common.

Figure 49:
LVDS Outputs DDR



Information

Bit width of the reference index and the stop result is configured by STOP_DATA_BITWIDTH and REF_INDEX_BITWIDTH

8.5.7 LVDS Output Test Pattern

Setting LVDS_TEST_PATTERN = 1 the interface continuously outputs the following fixed test patterns. All stop events are ignored.

Reference index = 111100001100110010101010bin (=15781034dec)

Stop result = 000010101010110011110000bin (= 699632dec)

Depending on the configuration of the output format width (REF_INDEX_BITWIDTH, STOP_DATA_BITWIDTH) only the corresponding lower bits of the reference index and the stop result are transmitted.

8.6 SPI Communication Interface

8.6.1 General

The SPI interface is implemented to

- Reset the chip to power on state
- Write configuration registers
- Verify configuration or status registers
- Initialize and restart measurements

- Byte-wise readout of results from the read registers (see Figure 31) via SPI instead via serial LVDS outputs

The serial interface is compatible with the 4-wire SPI standard in Motorola specification:

Clock Phase Bit = 1   Clock Polarity Bit = 0

8.6.2 Detailed Pin Description

- Pin SSN

The 'Slave Select Not' line is the HIGH-active reset for the serial interface. When set to LOW, the interface is ready for serial shift of data into or out of the device. Each access POR, INIT, READ or WRITE has to start with a positive pulse on SSN.

- Pin SCK

The 'Serial Clock' line is the driving clock which starts at LOW level and expects HIGH active pulses.

- Pin MOSI

The 'Master Out Slave In' line is the serial data input of the device. Data takeover is done with the falling edge of SCK. The MSB is sent first.

- Pin MISO

At 'Master In Slave Out' line, the serial data are clocked out of the chip with the rising edge of SCK. When SSN is set to HIGH, then the data output pin MISO is in high-Z state. The MSB is sent first.

- Pin INTERRUPT

A low level at the interrupt pin indicates to the receiving device that data are available.

8.6.3 Communication Commands (Opcodes)

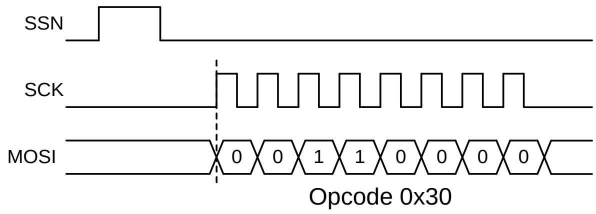
Figure 50:
Opcodes Overview

Opcode	Hex / BIN	Description
spiopc_power	0x30 = 0b00110000	Power on reset and stop measurement
spiopc_init	0x18 = 0b00011000	Initializes Chip and starts measurement
spiopc_write_config	0x80 = 0b100XXXXX	0x60 = 0b011XXXXX
spiopc_read_results	0x60 = 0b011XXXXX	Read opcode for result and status register X=8..31
spiopc_read_config	0x40 = 0b010XXXXX	Readout of configuration register X=0..17

- Power-ON Reset

After stabilization of all VDD33 and VDD18 the device expects the opcode spiopc_power = 0x30 to be sent via the SPI interface for power on reset. After the last bit of the opcode the reset remains active during $t_{HD,SSN}$ before the device is ready for the next read or write access. After the reset, the measurement is stopped and the configuration registers are set to internal defaults of the chip.

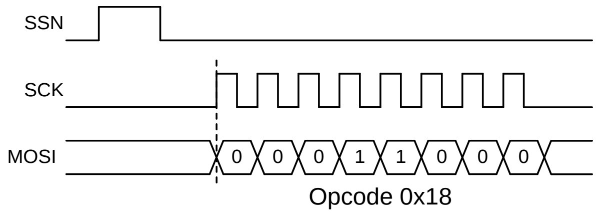
Figure 51:
Power-On Reset Opcode



- Initialization Reset

After the configuration, the initialization opcode spiopc_init = 0x18 resets again the chip to power on state, but preserves the configuration and starts the measurement. The initialization reset can be send while the reference clock or stops are applied. It takes 16 pulses of the reference clock before the stop channels are opened internally. After the initialization reset the delay t_{POR} has to be waited before next communication. The initialization reset can be applied also during measurements to restart the chip, but preserves measured data in FIFOs.

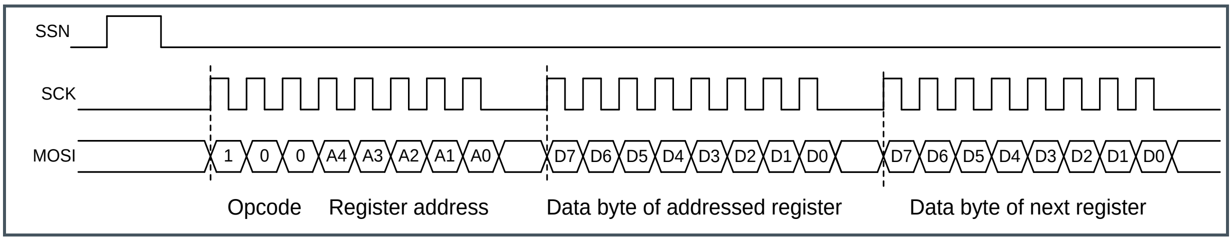
Figure 52:
Init Reset Opcode



- Write / Incremental Write

Write access is permitted to the configuration registers exclusively. The access starts by sending the opcode spiopc_write_config = 0x80 after a positive SSN pulse. The register address is just added to spiopc_write_config. The data are sent after the opcode. Incremental write access to the successive registers is possible by sending the next data bytes. A complete configuration starts normally at register 0, followed by all register data bytes.

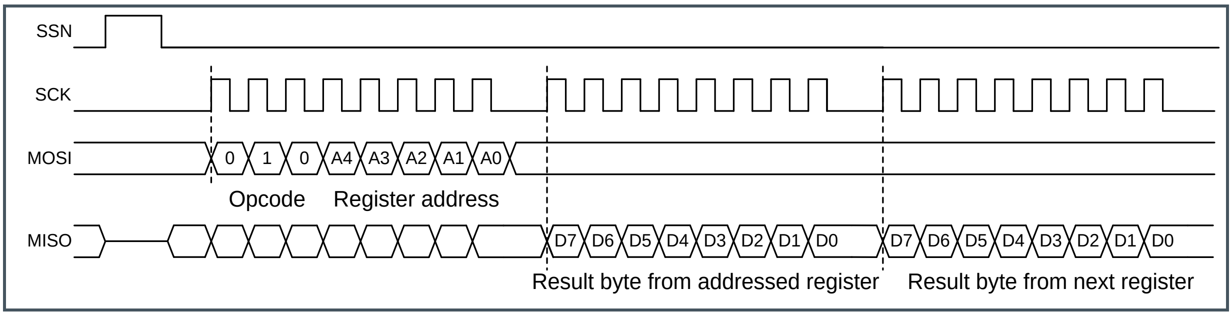
Figure 53:
SPI Incremental Write



- Read / Incremental Read

The read access to registers starts by sending the opcodes spiopc_read_results =0x60 or spiopc_read_config = 0x40 after a positive SSN pulse. The register address is just added to the opcode. After the opcode the data are clocked out at the MISO line. Incremental read access to following registers is possible by continuously reading bytes. Each register is suitable as start address for incremental access.

Figure 54:
SPI Incremental Read



8.6.4 Data Readout via SPI Interface

Reading results byte-wise from AS6501 e.g. by an external microcontroller is fully supported. While using the SPI interface, data read by LVDS has to be suppressed by setting PIN_ENA_LVDS_OUT to zero or at least by not applying a clock at LCLKIN.

When reading an empty channel the results of REFINDEX and STOPRESULT are marked with 0xFFFFFF. Typically, the measurement rate of AS6501 is much higher than the readout rate possible with SPI. In this case using COMMON_FIFO_READ and BLOCKWISE_FIFO_READ is helpful to get sequential results which were measured in parallel in AS6501.

REF_INDEX_BITWIDTH and STOP_DATA_BITWIDTH are not relevant for reading via SPI.

8.7 Coding of Results

8.7.1 Configuration of LSB by REFCLK_DIVISIONS

The reference clock period is divided into subdivisions by REFCLK_DIVISIONS for the definition of the LSB of the stop results at the output interface. One subdivision corresponds to the LSB and the stop results scale into multiples of this LSB. In order to avoid quantization artefacts of the output interface, the resulting LSB has to be much smaller than the single shot resolution of AS6501. The most convenient way is choosing an LSB of 1 ps by configuring REFCLK_DIVISIONS to the picosecond value of the reference clock period. Other LSB settings are possible as well, like LSB of 5 ps or 10 ps.

Figure 55:
LSB Configuration

Reference Clock Period	Reference Clock Frequency	REFCLK_ DIVISIONS LSB = 1 ps	REFCLK_ DIVISIONS LSB = 5 ps	REFCLK_ DIVISIONS LSB = 10 ps
500 ns	2 MHz	500000	100000	50000
250 ns	4 MHz	250000	50000	25000
200 ns	5 MHz	200000	40000	20000
100 ns	10 MHz	100000	20000	10000
80 ns	12.5 MHz	80000	16000	8000

Information

For LVDS output, REFCLK_DIVISIONS must not exceed the result bit width defined by STOP_DATA_BITWIDTH.

8.7.2 Examples for Codes of Time Measurements Results

Figure 56:
LSB Configuration

Readout of Stop Result		Resulting Stop Time with an Assumed LSB of			Note
Hexadecimal	Decimal	LSB = 1ps	LSB = 5ps	LSB = 10ps	
0x0	0	0 ps	0 ps	0 ps	
0x1	1	1 ps	5 ps	10 ps	
0x2	2	2 ps	10 ps	20 ps	
0xA	10	10 ps	50 ps	100 ps	
0x64	100	100 ps	500 ps	1000 ps	

Readout of Stop Result		Resulting Stop Time with an Assumed LSB of			Note	
Hexadecimal	Decimal	LSB = 1ps	LSB = 5ps	LSB = 10ps		
0x3E8	1000	1000 ps	5000 ps	10000 ps		
0x2710	10000	10000 ps	50000 ps	100000 ps		
0x61A7	24999	24999 ps	124995 ps	249990 ps	refclk-period t_{REFCLK} =250ns	
0xC34F	49999	49999 ps	249995 ps [2]	[1]		
0x3D08F	249999	249999 ps [2]	[1]	[1]		
0x1869F	99999	99999 ps	499995 ps	[1]	refclk-period t_{REFCLK} =1µs	
0x30D3F	199999	199999 ps	[1]	[1]		
0xF423F	999999	[1]	[1]	[1]		
0x3FFF	16383	16383 ps	81915 ps	163830 ps	refclk-period t_{REFCLK} =1µs	14 Bit
0xFFFF	65335	65335 ps	326675 ps	653350 ps		16 Bit
0x3FFFF	262143	262143 ps	[1]	[1]		18 Bit
0xFFFFF	1048575	1048575 ps	[1]	[1]		20 Bit
0x0FFFFF	1048575	1048575 ps	[1]	[1]	SPI: max readout with 20Bit [2]	

(1) Time difference exceed AS6501 specification for reference clock period
(2) REFCLK_DIVISIONS decreased by one is the highest possible readout value
(3) With SPI read-out the four upper bits are unused

8.7.3 Maximum Time Differences

The following table shows the maximum possible time differences between stops, depending on the reference index bit width.

Figure 57:
Maximum Time Differences

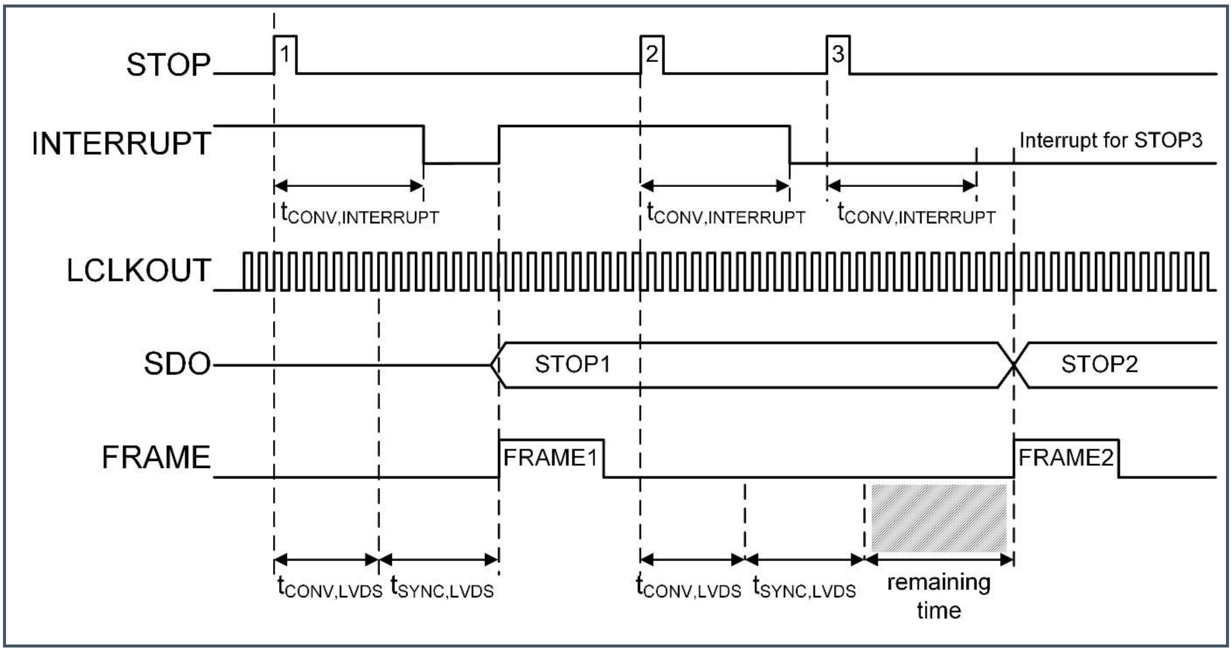
REF_ INDEX_ BITWIDTH	Mode	Maximum Readout Hexadecimal	Maximum Readout Decimal	Max. Time Difference with		
				f_{REFCLK} = 2 MHz	f_{REFCLK} = 5 MHz	f_{REFCLK} = 10 MHz
0 Bit	LVDS/SPI	No read-out	No read-out	0.5 µs	200 ns	100 ns
2 Bit	LVDS	0x3	3	2 µs	800 ns	400 ns
4 Bit	LVDS	0xF	15	8 µs	3.2 µs	1.6 µs
8 Bit	LVDS/SPI	0xFF	255	128 µs	51.2 µs	25.6 µs
16 Bit	LVDS/SPI	0xFFFF	65335	32 ms	13.0 ms	6.5 ms
24 Bit	LVDS	0xFFFFFF	16777215	8 s	3.2 s	1.6 s
6 Bit	LVDS	0x3F	63	31 µs	12.6 µs	6.3 µs

REF_ INDEX_ BITWIDTH	Mode	Maximum Readout Hexadecimal	Maximum Readout Decimal	Max. Time Difference with		
				f_{REFCLK} = 2 MHz	f_{REFCLK} = 5 MHz	f_{REFCLK} = 10 MHz
12 Bit	LVDS	0xFFF	4095	2 ms	800 µs	400 µs

8.8 Conversion Latency and Conversion Rate

The conversion latency t_{CONV} is the time need when an event at a stop input pin occurs until it is processed and ready for output through the interface. With LVDS instead of SPI output an additional synchronization latency to the LCLK is applied.

Figure 58:
Conversion Latency



The conversion and synchronization latency is only applied to single events. During an output sequence of several events the conversion latency is processed in parallel during the remaining time.

Converter Latency

The conversion latency t_{CONV} is the time needed when an event at a stop input pin occurs until it is processed. Once a stop event is recognized, it has to be converted into the results of TSTOP and REFID. The basic conversion latency t_{CONV} is the same for SPI or LVDS readout. After the conversion latency has passed, the INTERRUPT pin is set to zero (if not already zero from a previous stop) and the stop result is ready for readout via the SPI interface. The conversion latency depends also on the HIGH_RESOLUTION configuration.

LVDS Synchronization Latency

For both LVDS output modes, DDR+SDR, an additional synchronization latency t_{SYNC} has to be processed before the output sequence starts. With LVDS reading an additional latency t_{SYNC} for synchronization to the LCLK is applied. t_{SYNC} is counted in LVDS clock cycles and the output is indicated by setting the frame output pin.

8.9 Conversion Rate

Conversion rate is the rate where stop events can be measured. It is determined or limited by the peak input conversion rate or the read-out rate. The conversion rate of the stop events at the input can be higher or also lower than the read-out rate output interface. In any case, the FIFO will adapt a variable peak stop event rate and to the read-out rate.

8.9.1 Peak Conversion Rate

The peak input conversion rate is limited by the ability of AS6501 to sample, convert and store stop events in the FIFOs. The maximum peak conversion rate is limited minimal pulse-to-pulse-spacing tPPS of the chosen measuring mode. The number of conversions at peak conversion rate is given by the FIFO depth and to a certain extent by the read out rate of the interface.

8.9.2 Read-out Rate

The maximum read-out rate is reached when the output interface (either SPI or LVDS) is continuously in use for outputting the measurement results. The configured code length (LVDS: STOP_DATA_BITWIDTH and REF_INDEX_BITWIDTH, SPI: readout bytes) and the frequency define the readout capabilities.

8.9.3 Average Conversion Rate

The average conversion rate is determined either by the

- Peak input conversion rate: if the read-out rate is higher than peak input conversion rate no time event is getting lost because of a full FIFO. This is typically the case when reading out with LVDS.
- Read-out rate: if read-out rate is always slower than the input conversion rate then time measurements necessarily are getting lost because the FIFO may be full. This is typically the case when reading out via SPI. In this case the configuration of BLOCKWISE_FIFO_READ and COMMON_FIFO_READ is an option even to get measured a sequence of successive stops

8.9.4 Examples for Read-Out Rate with LVDS

The conversion rate of measured stop events can be calculated by dividing the bus frequency by the number of bits, which are readout reference index and stop result. The number of bits is configured by STOP_DATA_BITWIDTH and REF_INDEX_BITWIDTH.

Figure 59:
Example Data Average Conversion Rate

STOP_DATA_BITWIDTH	REF_INDEX_BITWIDTH	Sum of Bits	LCLK	SDR Throughput Rate	DDR Throughput Rate
00 (14Bit)	000 (0Bit)	14	300 MHz	21 MSPS	42 MSPS
00 (14Bit)	010 (4Bit)	18	300 MHz	16 MSPS	32 MSPS
01 (16Bit)	000 (0Bit)	16	300 MHz	18 MSPS	37 MSPS
01 (16Bit)	011 (8Bit)	24	300 MHz	12 MSPS	25 MSPS
10 (18Bit)	000 (0Bit)	18	200 MHz	11 MSPS	22 MSPS
10 (18Bit)	100 (16Bit)	32	200 MHz	6 MSPS	12 MSPS
11 (20Bit)	000 (0Bit)	20	100 MHz	5 MSPS	10 MSPS
11 (20Bit)	101 (24Bit)	44	100 MHz	2 MSPS	4 MSPS

Information

- Maximal throughput rate is only reached when the stop event rate at input is high enough.
- With CHANNEL_COMBINE = 1 (”Pulse Distance”) the throughput rate per stop input pin is doubled, as the stop events of one input pin are alternatively measured and readout by two channels.

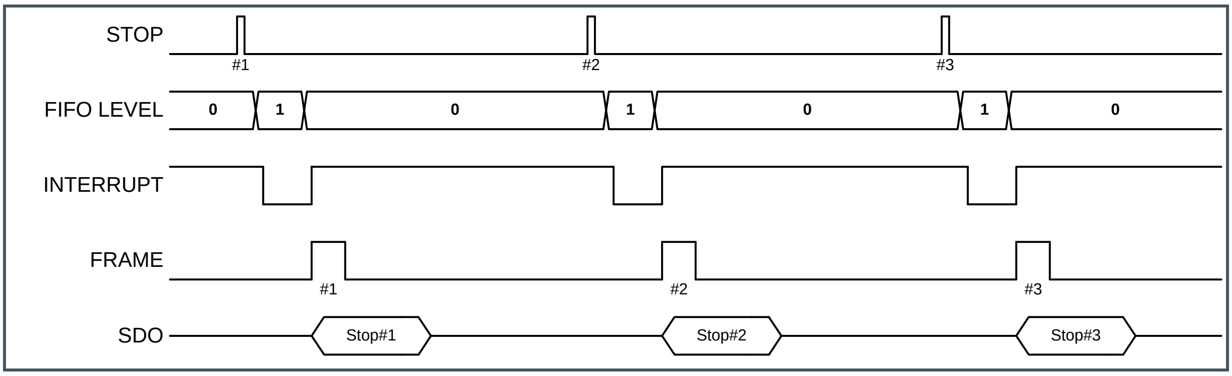
8.9.5 FIFOs for Adapting Peak and Average Conversion Rate

Each channel of AS6501 has a First-In-First-Out data buffer (FIFO). Generally, AS6501 is capable of measuring the incoming stops faster than the length of an output sequence. The FIFO is capable of storing up to data of 16 stop events until the data are read out. Up to a certain degree, the FIFO prevents rejection of stop events for a short time when the input stop event rate is higher than the read-out rate. But when the input data rate is constantly higher than the read-out rate, then the FIFO gets full and stop events are rejected. After a full FIFO was read out and empty space is available for stop measurement further two stops are needed to restart the FIFO ($t_{FIFO\_RESTART}$).

The maximum FIFO depth is 16, 8 or 4 stages, depending on the HIGH_RESOLUTION configuration (off, 2x, 4x).

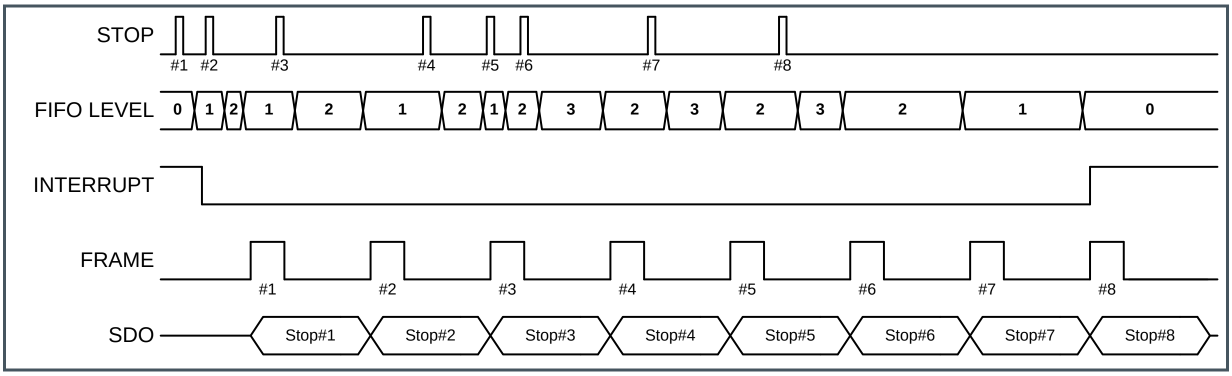
The following figures illustrate the typical dependencies between stop event rate and the read out rate. They are applicable for both SPI and LVDS readout. The INTERRUPT pin indicates that the result is available for read-out through the SPI interface. For SPI a continuous readout is assumed as long as the interrupt is on low level. For LVDS output the FRAME indicates the beginning of data output at SDO line. The interrupt goes back to HIGH when all FIFOs are empty even if output is LVDS. In the figures FIFO_DEPTH = 4 is assumed. The FIFO LEVEL indicates the stop event buffered in the FIFO. A stop event will increase FIFO LEVEL by one, reading out will decrease the FIFO LEVEL.

Figure 60:
Input Stop Event Rate Is Lower than the Readout Rate



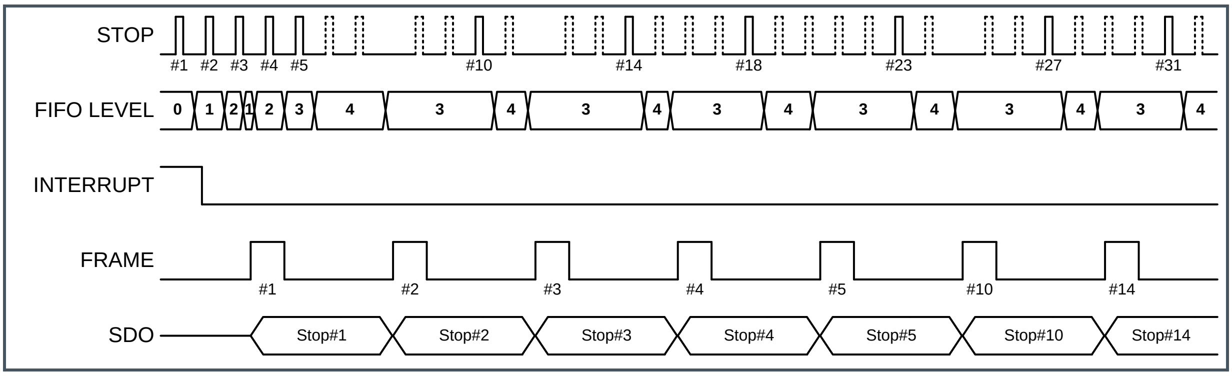
- Enough time for complete readout of first stop before the next stop event arises
- Interrupt goes back to high because the FIFO is empty after read-out
- In this example, no stop events are rejected. All stops are measured and read out

Figure 61:
Average Stop Event Rate Is Lower, but Peak Stop Event Rate Is Higher than the Readout Rate



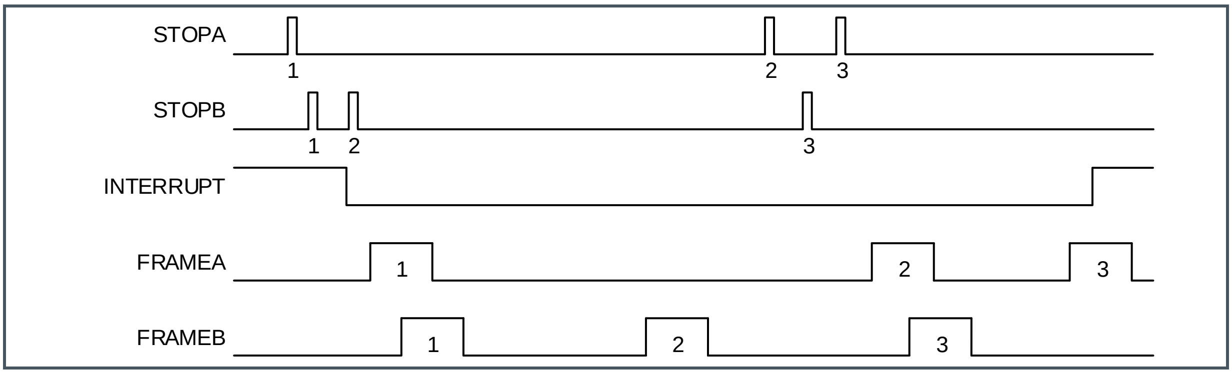
- Stop events during read-out are stored in FIFO
- Stop events buffer up to FIFO LEVEL 3
- In this example, no stop events are rejected. All stops are measured and read out.
- Interrupt goes back to high when all data are readout and the FIFO is empty.
- Maximal FIFO_DEPTH and HIGH_RESOLUTION limits the peak event storage

Figure 62:
Stop Event Rate Is Higher than the Readout Rate



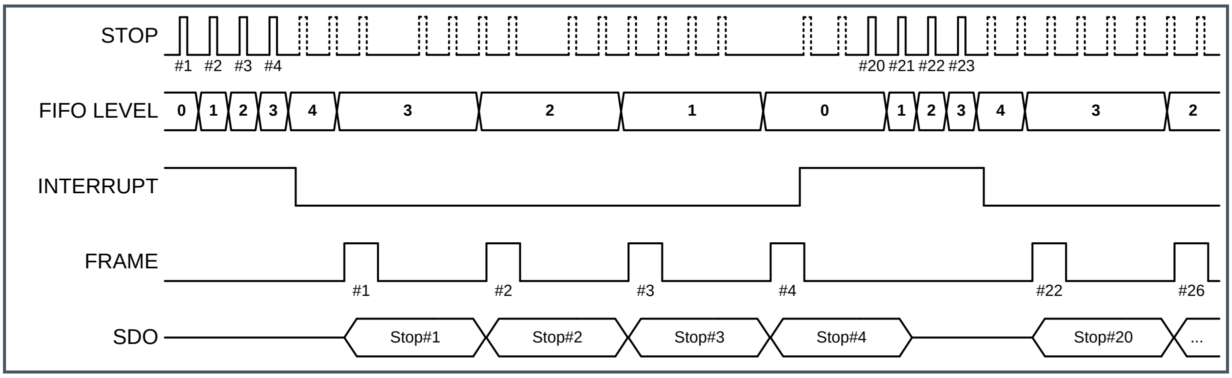
- During read-out stop events (dots) are ignored when FIFO full at FIFO LEVEL 4.
- After reading a result from a full FIFO the next two stops events (dashed) are still ignored but used to restart the FIFO
- Interrupt is always zero because the FIFO never gets empty.

Figure 63:
Stops On Both Channels



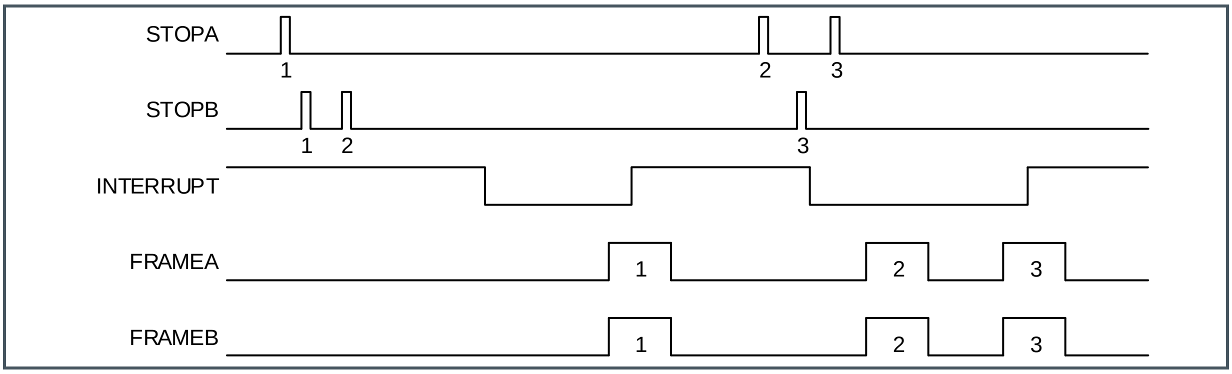
- Both channels are completely independent from each other (COMMON_FIFO_READ=0)
- In this example no stop events are rejected, because FIFOs never get full
- Interrupt remains zero as long as at least one FIFO has a valid data, interrupt gets high when all FIFO are empty

Figure 64:
BLOCKWISE_FIFO_READ



- A block of successive stop events are measured in a block before readout
- Readout of FIFO starts not before the FIFO is full.
- During read-out stop events (dots) are ignored when FIFO full at FIFO level 4…1.
- After reading all result from the FIFO the next two stops events (dashed) are still ignored but used to restart the FIFO
- Measurement starts not before the FIFO is empty.
- COMMON_FIFO_READ is applicable.

Figure 65:
COMMON_FIFO_READ



- All active FRAME pins are set simultaneously, as soon as all active FIFOs have value (COMMON_FIFO_READ = 1)
- As long as one FIFO has no valid data, no readout is done
- Interrupt doesn't fall to low before all active FIFOs have valid data
- In this example, no stop events are rejected, because FIFOs never get full.
- BLOCKWISE_FIFO_READ is fully applicable
- SPI readout only successively of both active FIFOs (A, B, A, B, …). It is not permitted to read one channel twice (e.g A, A, B, B, …)

9 Application Information

9.1 Configuration Examples

Typical configuration for LVDS:

```
org ROM_ADD_CFG    // config_default.cfg saved on 19.09.2016 11:58
equal 0x401F8535   // Register 3, 2, 1, 0
equal 0x43C0030D   // Register 7, 6, 5, 4
equal 0x0A0013A1   // Register 11, 10, 9, 8
equal 0x7DF1CCCC   // Register 15, 14, 13, 12
equal 0x00000000   // Register 19, 18, 17, 16
equal 0x00000000   // Register 23, 22, 21, 20
```

9.2 Example C++ Code

The following C++ code is provided to give an overview about how to organize the initial steps of a microprocessor, to be able to conduct a typical time measurement task with AS6501.

```
#include <uProcessor.h>
// This is an imaginary header file defined to support this example code
// -------------------------------------------------------------------------
// *** uProcessor.h ***
// -------------------------------------------------------------------------
// Almost every microprocessor has a specific C++ libraries (header files)
// that introduce
// specific commands for data readout. Therefore, this imaginary header data
// is given to support this example code.
// The intention of each virtual function on this header is clearly explained
// as follows.
// In real projects, instead of these functions, // the user should use the
// similar functions of the micro-processor which is used with AS6501.
// Virtual functions:
//    send_byte_to_SPI( Var1 );    : send Var1 (8 Bits) through the SPI
//    read_byte_from_SPI( Var1 ); : read 1 Byte data from SPI and write it
//    to Var1
// Virtual pin variables:
//      GPIO_SSN      : Variable (1 Bit) to control the output pin which is
//                      supposed to be connected the SSN pin of the AS6501
//      GPIO_INTERRUPT: Variable (1 Bit) to monitor the input pin which is
//                      supposed to be connected INTERRUPT pin of the AS6501
// -------------------------------------------------------------------------
// *** Configuration Registers ***
```

```
// ---------------------------------------------------------------------------
const char config_register[16] =
{35,85,1F,40,0D,03,C0,43,A1,13,00,0A,CC,CC,F1,7D,00};
// A typical config settings   = { config00, config01, … , config16 }
// ---------------------------------------------------------------------------
// *** SPI Opcodes ***
// ---------------------------------------------------------------------------
const char spiopc_power  = 0x30;  // opcode for "Power on Reset"
const char spiopc_init   = 0x18;  // opcode for "Initialize Chip and Start
                                  // Measurement"
const char spiopc_write_config = 0x80;  // opcode for "Write Configuration"
const char spiopc_read_config  = 0x40;  // opcode for "Read Configuration"
const char spiopc_read_results = 0x60;  // opcode for "Read Measure Results"
// ---------------------------------------------------------------------------
//    *** SPI Addresses ***
// ---------------------------------------------------------------------------
const char reference_index_ch1_byte3 = 8;
const char reference_index_ch1_byte2 = 9;
const char reference_index_ch1_byte1 = 10;
const char stopresult_ch1_byte3 = 11;
const char stopresult_ch1_byte2 = 12;
const char stopresult_ch1_byte1 = 13;
//   . . . .
const char stopresult_ch4_byte3 = 29;
const char stopresult_ch4_byte2 = 30;
const char stopresult_ch4_byte1 = 31;
// ---------------------------------------------------------------------------
// *** Other Variables ***
// ---------------------------------------------------------------------------
int  Buffer              = 0;   // buffer variable used to copy the SPI data
char i                   = 0;   // counter for for-loops
int  reference_index[4] = 0;   // reference index data array {Ch1, Ch2, Ch3,
                                // Ch4}
int  stopresult[4]      = 0;   // stop result data array {Ch1, Ch2, Ch3, Ch4}
bool config_error        = false; // flag that indicates if the config
                                  // registers are not written correctly
// -------------------------------------------------------------------------
// *** Main body of the software ***
// -------------------------------------------------------------------------
int main(void)
{
// -------------------------------------------------------------------------
// *** Power on reset ***
// -------------------------------------------------------------------------
    GPIO_SSN = 1;   // Reset the SPI interface and select the slave device
    GPIO_SSN = 0;

```

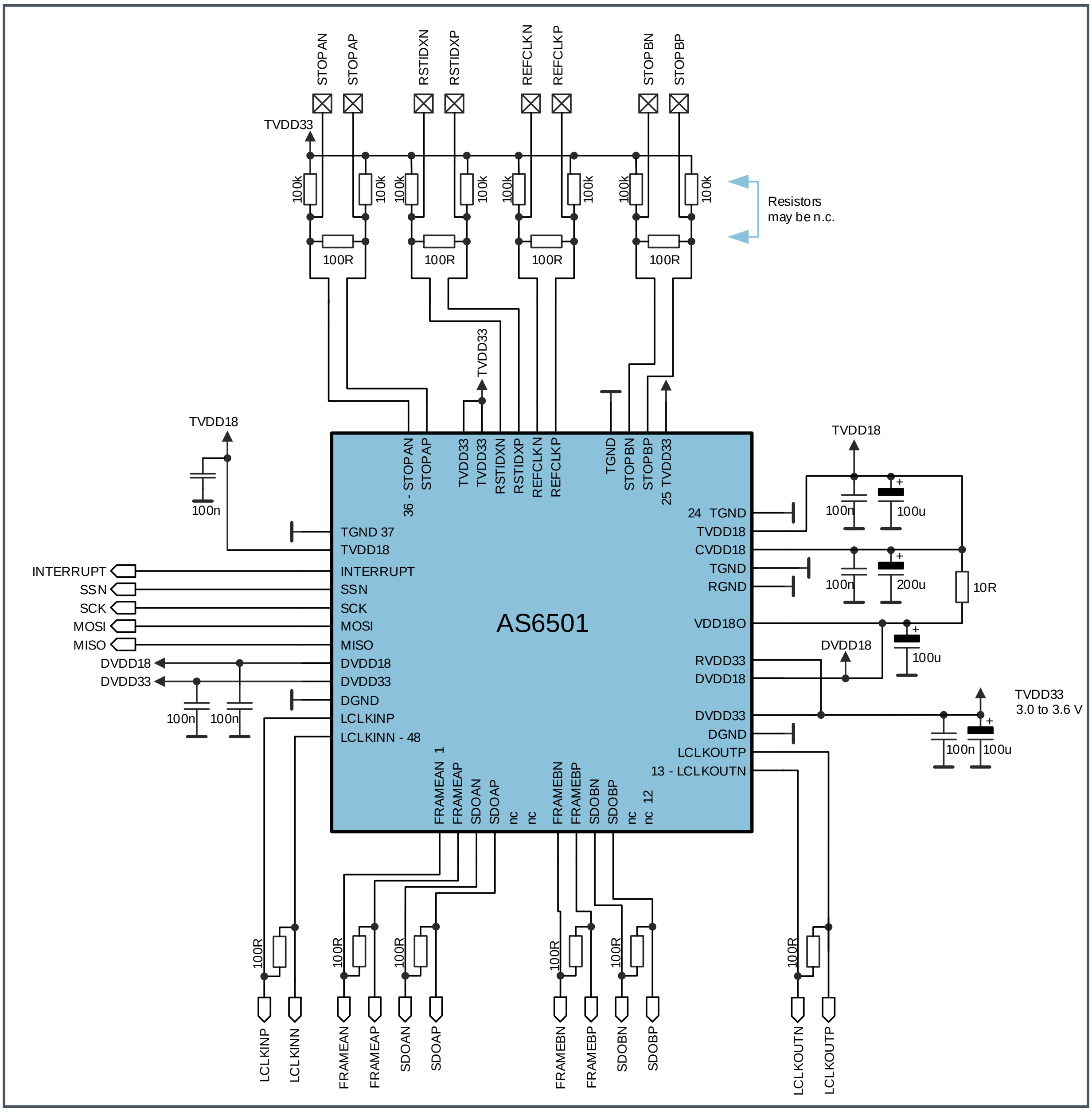
```
    send_byte_to_SPI( spiopc_power ); // Opcode for "Power On Reset" is sent
                                         // over SPI
// ------------------------------------------------------------------------
// *** Writing the configuration registers ***
// ------------------------------------------------------------------------
    GPIO_SSN = 1;   // Reset the SPI interface and select the slave device
    GPIO_SSN = 0;

    config_error = false;

    send_byte_to_SPI( spiopc_write_config + 00 );
// Opcode for "Write Configuration” and config address (00) are sent over SPI

    for ( i = 0; i < 17; i++)          // Send all 17 config registers via SPI
          send_byte_to_SPI( config_register[i] );
// ------------------------------------------------------------------------
// *** Verification of config registers ***
// ------------------------------------------------------------------------
    GPIO_SSN = 1;   // Reset the SPI interface and select the slave device
    GPIO_SSN = 0;

    send_byte_to_SPI( spiopc_read_config + 00 );
// Opcode for "Read Configuration"  and config address (00) are sent over SPI

    for ( i = 0; i < 17; i++)
    {
       read_byte_from_SPI( Buffer ); // read byte from SPI to Buffer variable

        if ( config_register[i] != Buffer ) config_error = true;
// if there was a failure in writing the config registers, then the
// config_error flag is raised.
    }
// ------------------------------------------------------------------------
// *** Initialize and start the measurement ***
// ------------------------------------------------------------------------
    if (config_error == false )
    {
        GPIO_SSN = 1;   // Reset SPI interface and select the slave device
        GPIO_SSN = 0;

        send_byte_to_SPI( spiopc_init );
// Opcode for "Initialize" is sent over SPI. This is required to start
// measuring process
// ------------------------------------------------------------------------
// End of the configuration settings. After now the time measurement will
// start. This code is designed to use SPI to read the measurement data from
// AS6501. Using LVDS as a output interface requires additional hardware
```

```
// ------------------------------------------------------------------------
// *** Readout of measurement data via SPI ***
// ------------------------------------------------------------------------
        while( GPIO_INTERRUPT != 0 ); // wait till the Interrupt pin is low

        GPIO_SSN = 1;    // Reset SPI interface and select the slave device
        GPIO_SSN = 0;

        send_byte_to_SPI( spiopc_read_results + reference_index_ch1_byte3 );
             // Opcode for "Read Result" and data address are sent
        for ( i = 0; i < 4; i++)
        {
            read_byte_from_SPI( Buffer ); // read one byte from SPI to Buffer
            reference_index[i] = reference_index[i] + ( Buffer << 16 );
// Data is shifted 16 Bits to the left and added to the reference_index
            read_byte_from_SPI( Buffer ); // read one byte from SPI to Buffer
            reference_index[i] = reference_index[i] + ( Buffer << 8 );
// Data is shifted 8 Bits to the left and added to the reference_index
            read_byte_from_SPI( Buffer ); // read one byte from SPI to Buffer
            reference_index[i] = reference_index[i] + Buffer;
// Data is directly added to reference_index
// The complete reference index (3 Bytes) has been received.
            read_byte_from_SPI( Buffer ); // Same process as reference_index
            stopresult[i] = stopresult[i] // is repeated for stop results
                            + ( Buffer << 16 );

            read_byte_from_SPI( Buffer );
            stopresult[i] = stopresult[i] + ( Buffer << 8 );

            read_byte_from_SPI( Buffer );
            stopresult[i] = stopresult[i] + Buffer;
// The complete stop result (3 Bytes) has been received
        }
        // In this point the software has obtained
        // the reference_index and stopresult data for all channels,
        // the rest of the codes should be designed depending on the user’s
        // application.
        // . . .
    }
        // . . .
}
```

9.3 Schematic

The following figure shows a typical circuit with power supply and line termination.

Figure 66:
Schematics for LVDS Inputs and Outputs



9.4 External Components

Supply Decoupling: AS6501 provides 6 power supply domains. Carful buffering is recommended. Small decoupling capacitors (e.g. 100nF) with minimal ESL and ESR help to filter external power supply noise when placed near to the power supply pins. The optimum number of decoupling capacitors depends on the actual application.

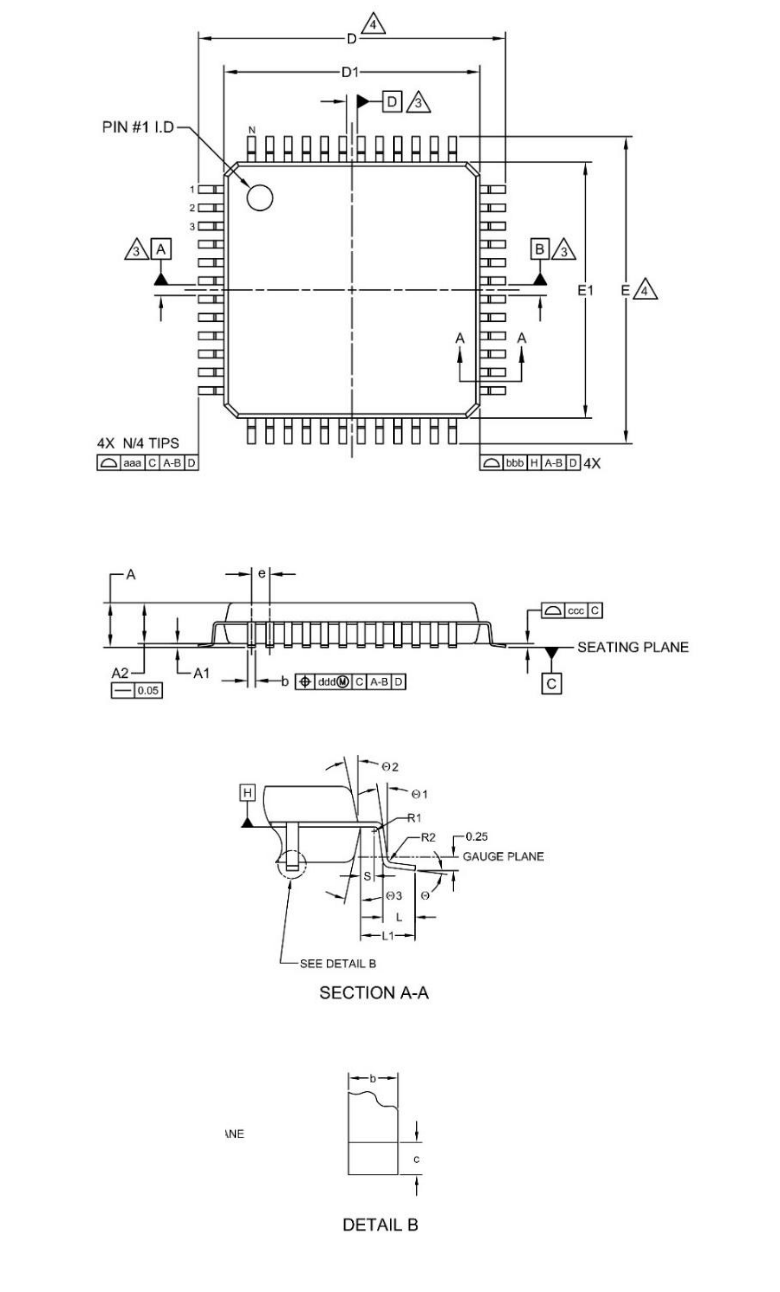
It is recommended to use separate supplies for time-analog (TVDD33) and digital (DVDD33, RVDD33) supply pins to isolate digital switching noise from sensitive circuitry. In case only a single (digital) supply is available, it should be routed to DVDD33 and RVDD33. It can then be tapped and isolated with a resistor (10 Ohm) to TVDD33.

Grounding: A single ground plane is sufficient to give optimum performance, provided the analog, digital and clock sections of the board are cleanly partitioned.

Signal Lines: Even though LVDS signalizing on input and output reduces ground bounding during its transition, the positive and negative signal path has to be well matched and their trace should be kept as short as possible. Time-analog signal path like single ended (CMOS) stop inputs must be treated as a transmission line and should have a solid ground return path with a small loop. A serial resistor (10 Ohm) in single ended (CMOS) signal lines further help to damp reflections.

10 Package Drawings & Markings

Figure 67:
QFP48 Package Outline Drawing



Ref.	Min	Nom	Max
A			1.60
A1	0.005		0.15
A2	1.35	1.40	1.45
B	0.17	0.22	0.27
C	0.09		0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1, R2	0.08		0.20
S	0.20		
Θ	0°	3.5°	7°
Θ1	0°		
Θ2, Θ3	11°	12°	13°
aaa, bbb		0.20	
ccc, ddd		0.08	
N	48		

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

Figure 68:
QFP48 Package Marking/Code

YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

11 Reel Information

The device will be shipped in a JEDEC 7'' tape.

12 Soldering & Storage Information

Figure 69:
Solder Reflow Profile Graph

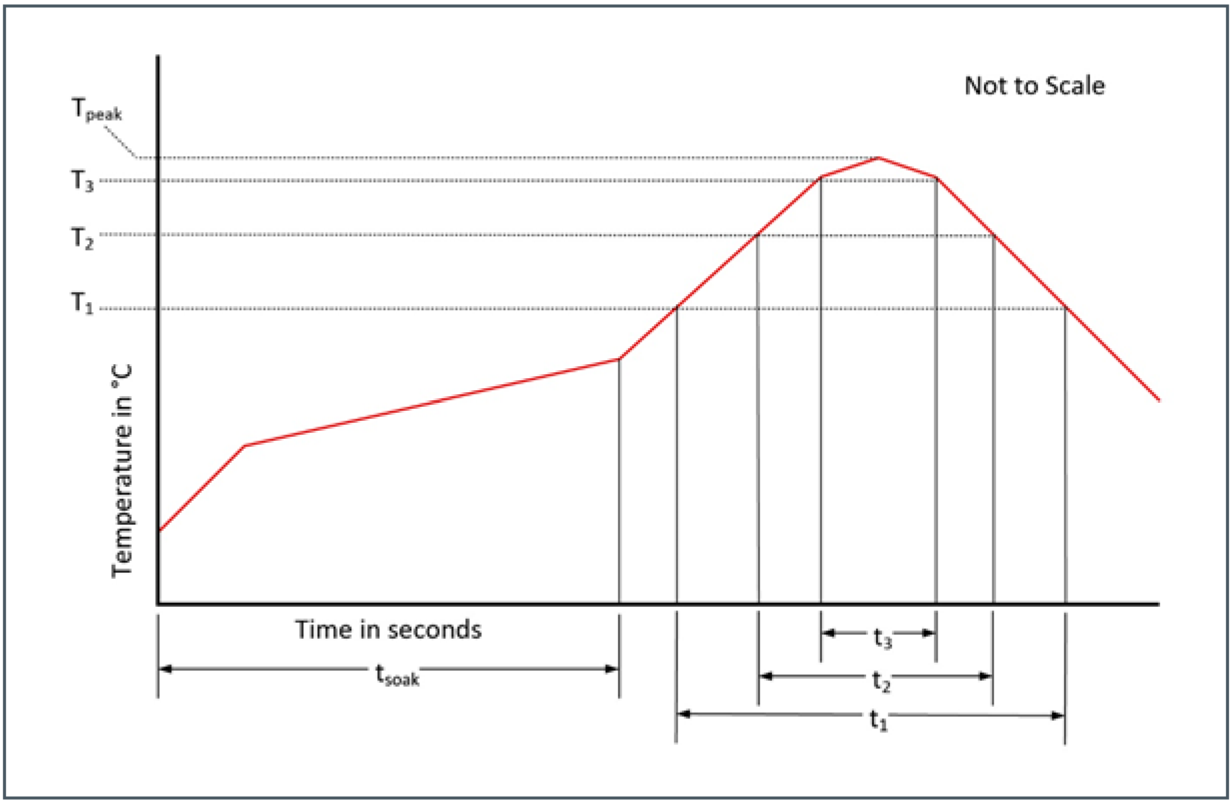


Figure 70:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

13 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ScioSense B.V. standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

1.

Changes from previous version to current revision v3-00	Page
Schematic drawing corrected, pin 28, pin 25 net name	56

2.

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

14 Legal Information

RoHS Compliant & ScioSense Green Statement

RoHS Compliant: The term RoHS compliant means that ScioSense B.V. products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ScioSense Green (RoHS compliant and no Sb/Br): ScioSense Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ScioSense B.V. knowledge and belief as of the date that it is provided. ScioSense B.V. bases its knowledge and belief on information provided by third parties and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ScioSense B.V. has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ScioSense B.V. and ScioSense B.V. suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.