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Time-to-Digital-Converter

Application Note

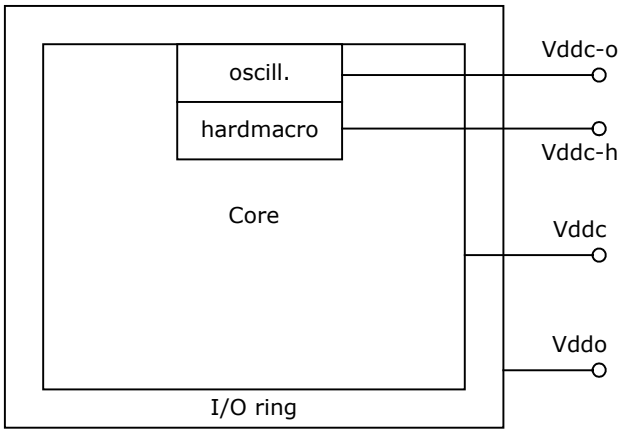
TDC-GPX
PLL Regulation Circuits

16th September 2010
Document-No.: AN013_e V3.0

Introduction:

The TDC-GPX chip shows different blocks with separate power supplies:

Figure 1 TDC-GPX power supply blocks



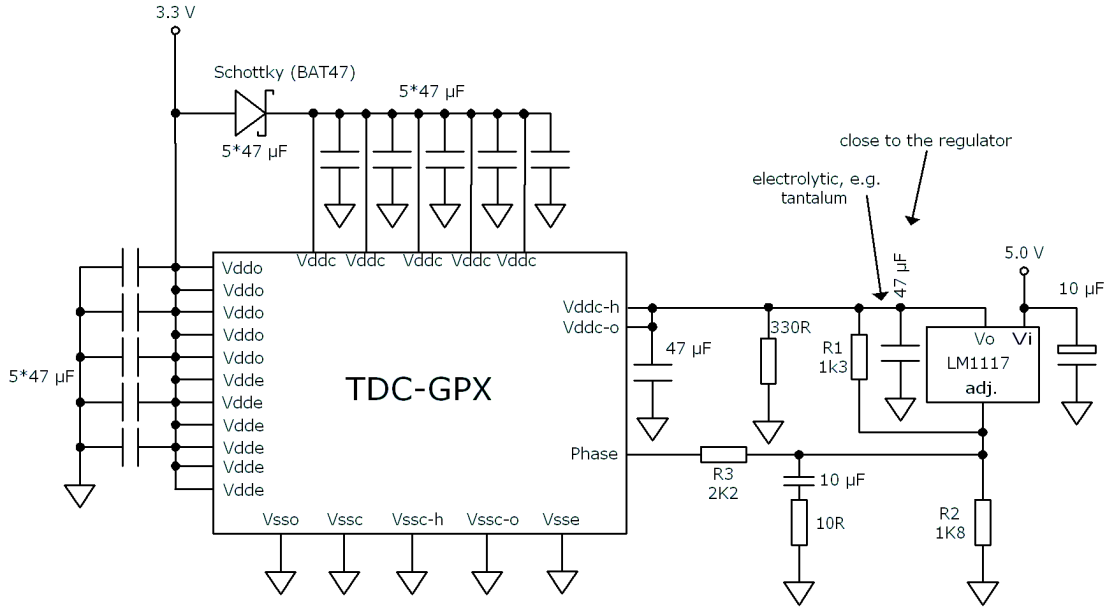
- Vddc-o,Vddc-h Oscillator and Hardmacro
  This is the time interval measuring unit
- Vddc Core
  All digital circuitry besides the measuring unit (ALU, FIFO's etc.)
- Vddo,Vdde I/O Padring and LVPECL input buffers I/O buffers, input protection

The purpose of the PLL regulation circuit is to keep the speed of the oscillator & hardmacro constant by regulating the voltage Vddc-o/h between 2.4 and 3.6V.

Note:

The recommended circuit is based on the LM1117. We strongly recommend to use only LM317 or LM1117 regulators. Only for these regulators the ciruit is tested and approved. Do not use low-drop regulators. This regulator's reference refers to the output voltage.

Figure 2: Circuit with one regulator and Schottky diode



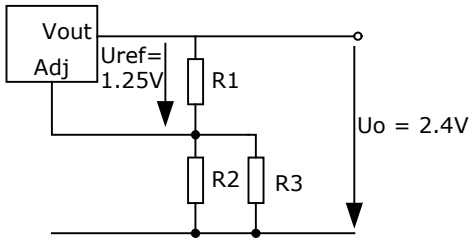
The IO buffers are supplied with 3.3V typically to be compatible with a 3.3V design. It is strongly recommended to use a linear regulator to provide the 3.3V. Switched mode regulators will introduce a lot of noise to the measurement. The core voltage is set to 3.0V. The easiest way to do this is to use a BAT47 schottky diode. The purpose is to avoid voltage differences bigger than 0.6V between Vddc and Vddo on the one side and Vddc and Vddc-o/h on the other.

The outputs' high-side switches do not fully close when Vddc is more than 0.6V below Vddo. Therefore other devices on the bus must be able to drive a few mA to pull the outputs down to LOW. This may be no problem for an FPGA and only one TDC-GPX connected to the bus. But of course this is a problem with weak drivers and more than one device on a bus.

Calculating the Resistors

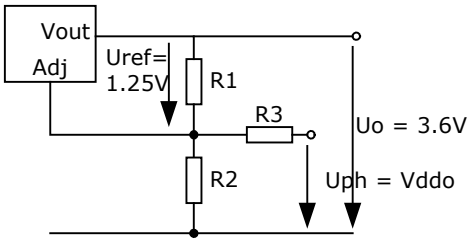
In the TDC-GPX application we look at two extremes:

1. Phase output has 0% duty cycle -> Low output voltage. In this case R2 and R3 are in parallel (R23).



NegPhase = 1:
Uph=0 -> Uo = Low

2. Phase output has 100% duty cycle -> High output voltage. In this case R3 is at Vddo.



NegPhase = 1:
Uph=Vddo -> Uo = High

For given resistor values the output levels are:

$$U_{min} = U_{ref} \times \left(1 + \frac{R_2}{R_1}\right) \qquad \frac{1}{R_{23}} = \frac{1}{R_2} + \frac{1}{R_3}$$

$$U_{max} = U_{ref} \times R_{23} \times \left(\frac{1}{R_1} + \frac{1}{R_{23}}\right) + U_{ddo} \times \frac{R_{23}}{R_3}$$

For given voltage levels the resistor are calculated like:

$$R_3 = \frac{U_{ddo}}{(U_{max} - U_{min})}\left(\frac{U_{min}}{U_{ref}} - 1\right) \times R_1$$

$$R_2 = \frac{U_{ddo}}{(U_{ddo} - U_{max} + U_{min})}\left(\frac{U_{min}}{U_{ref}} - 1\right) \times R_1$$

Blocking Capacitors

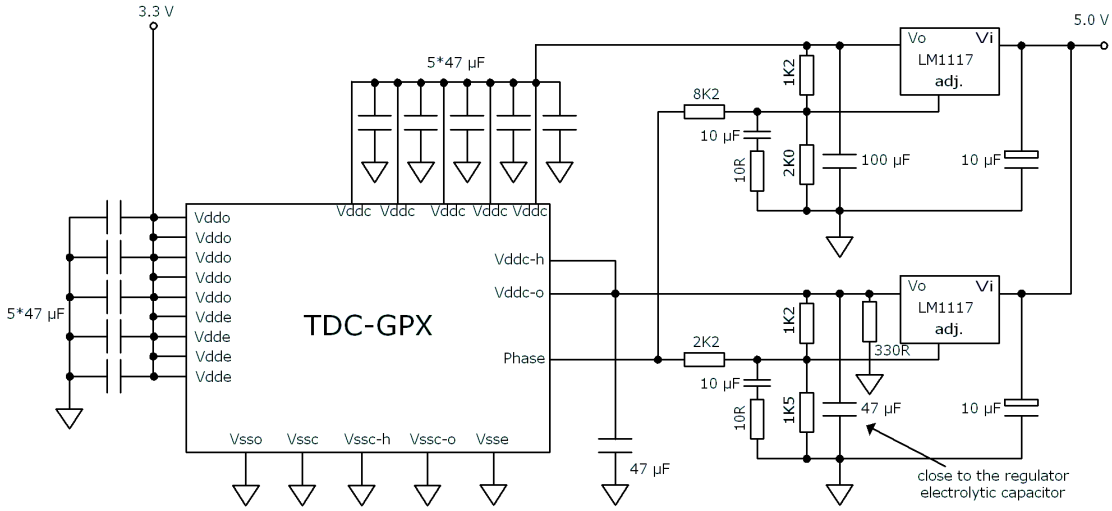
1.	Vddo	Data bus I/O supply	TQFP pins 17, 40, 54 FBGA pins G3, L6, L12	100 nF per pin
2.	Vddo	I/O supply	TQFP pins 2,98,94,91,86,82,81,77 FBGA pins B1,A3,C4,C5,B7,A9,B9,A11	Connect all pins to a common copper plane and place two 100nF capacitors close to pins 77/A11 and 98/A3
3.	Vddc	Core supply	TQFP pins 1, 10, 39, 69, 79 FBGA pins A1, F1, M7, E12, B10	Connect a capacitor to each side of the chip TQFP pins 10, 39, 69, 79 FBGA pins F1, M7, E12, B10
			Standard: 4 x 47 µF Derating (increase of standard deviation) with smaller capacities: 4 x 10 µF up to 200ns: no effect up to 500ns: about 4ps up to 1000ns: about 15ps 4 x 22 µF up to 200ns: no effect up to 500ns: about 2 ps up to 1000ns: about 7 ps	
4.	Vddc-o Vddc-h	Hardmacro supply	TQFP pins 87, 88 FBGA pins C6, A7	One capacitor to each pin and the voltage regulator output
			Standard: 1 x 47 µF at regulator out and 1 x 47 µF at the pins. The regulator decoupling can be reduced to 10 µF without a negative effect Derating (increase of standard deviation) with smaller capacities at the pins: 2 x 10 µF up to 200ns: no effect up to 500ns: about 4 ps up to 1000ns: about 10 ps 2 x 22 µF up to 200ns: no effect up to 500ns: about 2 ps up to 1000ns: about 5 ps	

Extended Regulation Range

The solution from above shows a slightly reduced regulation range. The reason is that the oscillator speed at Vddc-o/h = 3.6V & Vddc = 3.0V is a little bit less than with both voltages at 3.6V.

There is a solution to overcome this: using a second regulation circuit for Vddc instead of the schottky diode. The second regulator for Vddc has a regulation range from 3.0V to 3.6V. In other words: With TDC-GPX output phase=LOW regulator 1 delivers Vddc-o/h = 2.4V and regulator 2 delivers Vddc=3.0V. At phase=HIGH regulator 1 delivers Vddc-o/h = 3.6V and regulator 2 delivers Vddc=3.6V. Of course the circuit is alittle bit more complex.

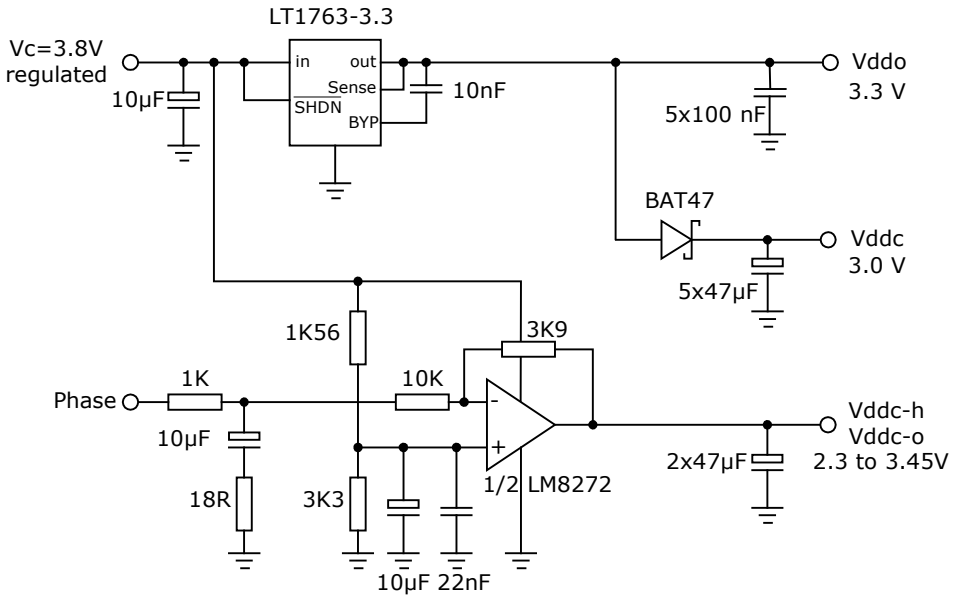
Figure 3 Circuit with two regulators for extended regulation range



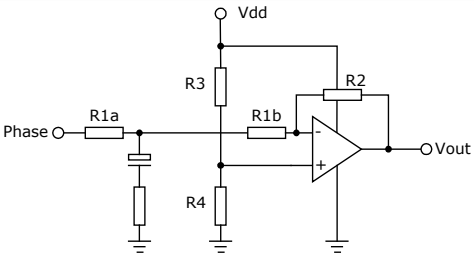
Low-drop Solution

The recommended circuit from above doesn't work with low-drop regulators. In applications where the power dissipation has to be as low as possible the following circuit can be used. In this circuit the voltage regulator is replaced by an operational amplifier.

Figure 4: Low drop solution



The LM8272 has enough output power and is ecspecially designed to drive high capacitive loads.

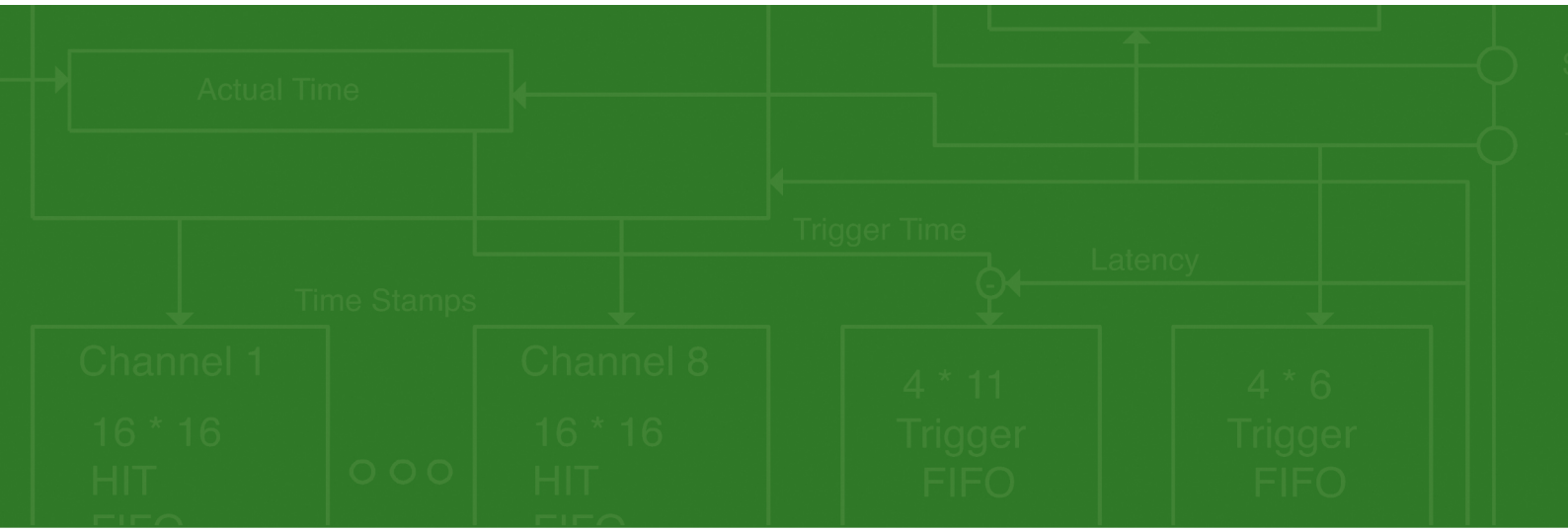


$$V_{phase} = V_{ddo}$$

$$U_{out} = U_d \left(1 + \frac{R_2}{R_1}\right) \frac{R_4}{R_3 + R_4} - U_{phase} \frac{R_2}{R_1}$$

$$\frac{R_2}{R_1} = \frac{U_{max} - U_{min}}{U_{phase}}$$

$$\frac{R_3}{R_4} = \frac{U_d \times (U_{phase} + U_{max} - U_{min})}{U_{max} \times U_{phase}} - 1$$



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